Exhibit 18

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00615[1]
Patent No. 7,619,912

PATENT OWNER RESPONSE

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[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00203 and have been joined as petitioners in this proceeding.

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I. INTRODUCTION[2]

For reasons stated below, Petitioner has not met its burden to prove the unpatentability of claim 16.

II. BACKGROUND

A. Summary of the '912 Patent

Claim 16 involves a concept called rank multiplication in registered DDR DRAM modules. A DDR DRAM module contains DDR devices arranged in "ranks" on a printed circuit board ("PCB"). *Id.* at 1:26-31. At the time of the invention, most computer systems supported accessing only one or two ranks per memory module. EX1001, 1:20-2:42.

Rank multiplication allows expansion of memory capacity by presenting a DDR DRAM module having *e.g.*, 2n physical ranks of memory devices as a module with n (virtual) ranks to the computer system. *Id.*, 6:64-7:19. In this way, "even though the memory module 10 actually has the first number of [physical] ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of [logical or virtual] ranks of memory devices 30." *Id.*, 7:9-13.

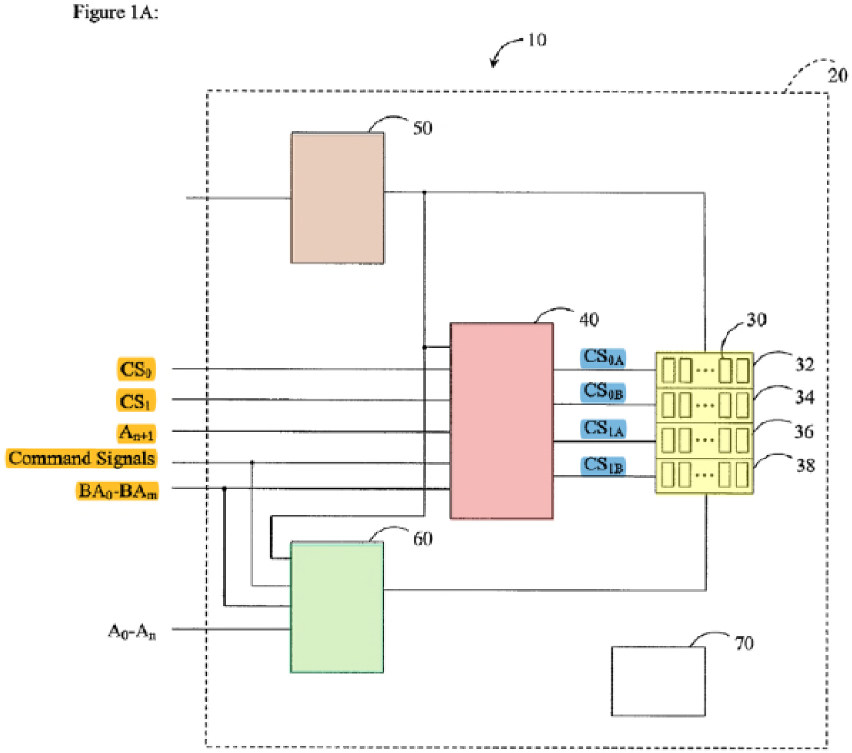
Rank multiplication also enables constructing DRAM modules of a given capacity using lower density memory devices that could cost less. *Id.*, 4:42-58, 22:5-

[2] All emphases are added unless otherwise noted.

14. For example, for the same 1 GB memory capacity, it could be more cost-effective to use thirty-six 256-Mb DRAMs arranged in 4 ranks than eighteen 512-Mb DRAMs arranged in two ranks. *Id.*, 4:42-58, 4:59-5:5.

Figure 1A illustrates an example of a DDR DRAM module with rank multiplication capability. The memory module has a register 60 and a logic element 40.

Figure 1A:



The logic element receives a set of input control signals from the computer system that include chip-select signals CS_0-CS_1, address signal A_{n+1}, and bank address signals BA_0-BA_m. *Id.*, 7:35-53; Fig. 1A. From the computer system's perspective, it is connected to two ranks of memory devices selectable by CS_0 or

CS_1, even though the memory devices are arranged in four physical ranks. *Id.*, 6:55-7:19. In response to the received input control signals, the logic element on the DDR DRAM module generates a set of output control signals, corresponding to the four physical ranks of the memory devices. *Id.*, 6:61-63. The logic element 40 also receives command signals (such as read/write) from the computer system. *Id.*, 6:55-61, 7:46-53. In response to the command signals and the input signals, the logic element transmits the command signals to the memory devices on the selected rank of the DDR DRAM module. *Id.* In some embodiments, command signals are transmitted to only one memory device in a rank at a time. *Id.*, p.44, 3:9-43.

B. Claim 16 Was Repeatedly Confirmed

Claim 16 was affirmed without amendment multiple times during the decade-long, rigorous *inter partes* reexamination by the Examiner, the Board and the Federal Circuit. On April 4, 2011 the Examiner affirmed the validity of claim 16. EX1010, 1402-03, 1405. Later, the Examiner again affirmed the validity of claim 16 despite third-party requesters' objections. *Id.*, 3865-67, 3904, 4442, 4828, 4830, 4702-04, 4723-25. The Board twice affirmed the Examiner's maintenance of claim 16. EX1011, 78-80, 152. The Federal Circuit affirmed the Board's decision. *Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. 2020). As discussed below, these decisions applied a construction of "rank" that Patent Owner respectfully submits the Board is legally bound to follow.

III. SKILL LEVEL OF A POSITA

Patent Owner applies the skill level proposed by Petitioner for this proceeding.

IV. CLAIM CONSTRUCTION

The term "rank" should be construed as "a predetermined set of DRAMs on a memory module that act together to send or receive a fixed number of data bits via a fixed width data bus, in response to a read or write command and independently from other DRAMs on the memory module." Previously, Netlist also agreed to the following construction: "***a group of memory devices*** enabled to receive and transmit data by a common chip-select signal." EX2026, 7. For the purpose of this action, the one issue that the Board needs to resolve is whether "rank" can include just "one memory device." Such an interpretation is inconsistent with the disclosure of the '912 patent and the repeated admissions of Petitioners.

A. The Intrinsic Evidence Does Not Support a Single-DDR-Device Rank Construction

Claim 16 is directed to a memory module having "a first[/second] number of DDR memory devices arranged in a first[/second] number of ranks."[3] "DDR" refers

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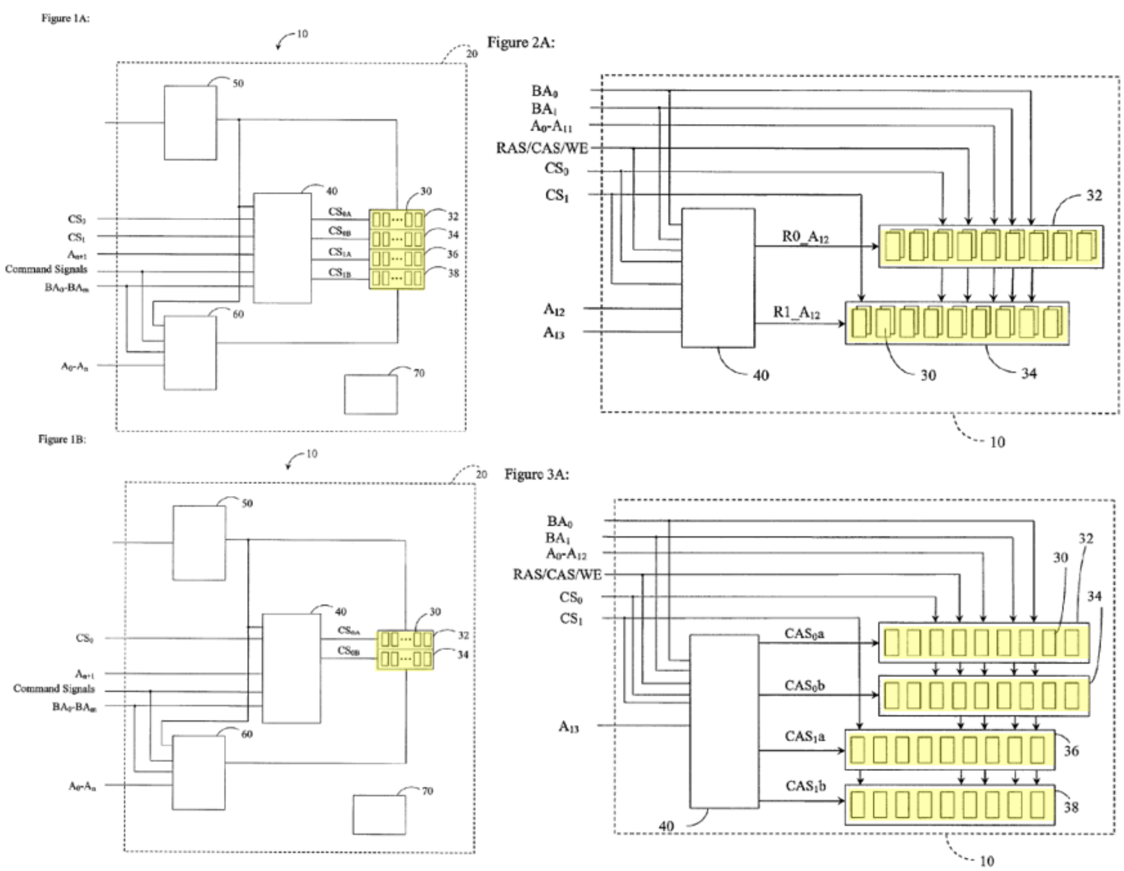
[3] Petitioner's proposed construction acknowledges that "rank" is for a memory module. Pet. 12 (arguing "rank" is "an independent set of one or more memory devices ***on a memory module*** ….").

to "double-data rate," a type of memory standardized by JEDEC. EX1033, 332-333. The '912 patent repeatedly and consistently references ranks composed of multiple memory devices. EX1001, 12:13-25 ("simulate ***a single rank of memory devices*** having twice the memory density"); 7:55-8:43, 8:64-9:18 (logic tables "for the selection among ranks of memory devices 30"). The figures also consistently show multiple DDR memory devices in each rank. *See id*., Fig. 1A-B & 6:31-38, 2A, 3A (reproduced below, in which each rank 32, 34, 36 or 38 has multiple devices as depicted).



The specification distinguishes embodiments that "multipl[y] memory

devices per rank" (*e.g.*, Figs. 1C, 2A) from embodiments that "multipl[y] the number of ranks per memory module" (*e.g.*, Figs. 1A-1B, 3A). *Compare* EX1001, 12:12-15 ("In certain embodiments, ***two memory devices*** having a memory density are used to simulate a ***single memory device*** having twice the memory density") & 12:36-37 *with* 12:15-21 ("in certain embodiments, two ***ranks of memory devices*** having a memory density are used to simulate ***a single rank of memory devices*** having twice the memory density") & 12:37-38.

The '912 patent also teaches that, "[t]he DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width," for example, 64 or 72 bits. EX1001, 2:16-22. As Dr. Brogioli explains, a POSITA would understand the width of a "rank" of DDRs corresponds to a fixed number of data bits received via a fixed width data bus, which corresponded to the full bit-width of a memory module at the time of the invention. EX2062 ("Brogioli"), ¶¶112-113, 113 n.3.

Petitioner argues that the '912 patent describes a single-device "rank" embodiment. Pet., 12-13. The cited passage states "[i]n certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of ***Table 1***). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time." EX1001, 8:47-54.

As Dr. Brogioli explains, when read in context of the entire specification, this passage would not be understood to refer to single-device ranks. Brogioli, ¶¶105-107. As provided in Table 1, during State 4, only the rank corresponding to CS_{1A} is chosen. EX1001, 7:60-8:33. Read in context, the embodiments described with reference to Table 1 refer to transmitting a command signal to one of the multiple memory devices in the selected rank (*i.e.*, one of at least two memory devices in the rank corresponding to CS_{1A}). Brogioli, ¶¶106-107; *see also* EX1001, Example 2 Verilog (gated CAS signal sent to a single device in the rank through control of en_fet_a or en_fet_b (FET switches for a single device a/b)). This is because Table 1 is described as "a logic table … for the selection among <u>ranks</u> of ***memory devices 30*** using chip-select signals." *Id.*, 7:56-59. The "memory device**<u>s</u>** 30" are consistently described throughout the specification as part of multi-device ranks. Brogioli, ¶¶106-107; 6:31-38, 20:64-65, 22:34-35; Figs. 1A, 1B, 2A, 3A. Thus, a POSITA would understand the passage as referencing a memory module with at least two ranks, each rank having at least two memory devices. Brogioli, ¶107.

Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1

Petitioner further argues that disclosures in the '215 patent suggests "that a

'rank' just requires 'at least one … memory integrated circuit.'" Paper 14 at 5 (citing '215 patent, 3:33-35, 37:35-38). The context of that disclosure is provided below.

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;

a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and

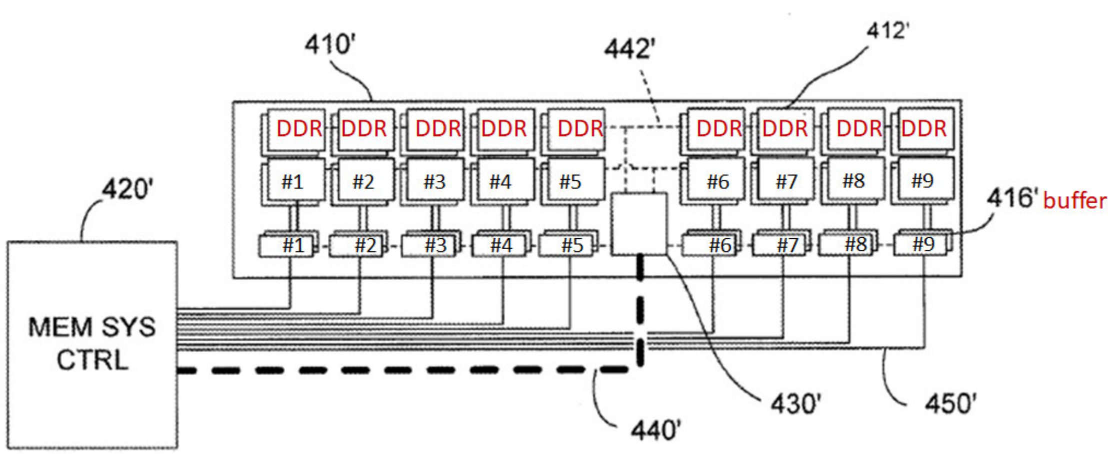
logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

(EX2038 cl. 1, col. 37)

In certain embodiments, the printed circuit board has a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system. The register is configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command. The plurality of memory integrated circuits are arranged in a plurality of ranks including a first rank and a second rank, and including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank. The first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command. The second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command.

(EX2038, p.187, 3:25-43)

There are several issues with the argument. First, the disclosure does not appear in the '912 patent. Second, the disclosures for "at least one … memory integrated circuit" in the '215 patent do not define the term "rank." If "rank" in its plain meaning includes only one memory integrated circuit, the language "at least one . . . memory integrated circuit" would be redundant. The purpose of this language is to focus on what is done with at least one of the memory integrated circuits in the rank vis a vis the buffer subsequently described. Specifically, it provides context that a claimed "buffer" can be, but need not be, coupled to multiple memory devices per rank. *See* illustration below and EX2038, Figs. 5A-5B, 8:66-9:3 ("one or more switches 120 …to selectively couple one or more data signal lines to a common data signal line"). That is, the buffer can be coupled to just "one" memory IC in the rank. *Id.*



The '215 claim also specifies that the buffer, in response to a memory command, "enable[s] communication of the first[/second] data burst between the at

least one first[/second] memory integrated circuit" and the memory controller. EX2038, 37:54-56, 37:59-61 (highlighted in green). The '215 specification is in accord, with the sentences immediately following Samsung's quoted language (yellow) referencing the first and second data burst (green). *Id.*, 3:25-53. The language in yellow provides the context for later-recited first/second memory ICs and their structures and functions, and does not define "rank."

B. Petitioner's Admissions Confirm Patent Owner's Construction of Rank

Petitioners' proposed construction contradicts the definitions of "rank" that Petitioners advance outside this proceeding. For instance, in IPR2022-00063, Samsung asserted that "[t]he term 'rank' should be construed to mean an independent set of memory device*s* [plural] that act together in response to a memory command … to read or write the full bit-width of the memory module." EX2055, 13. As another example, Samsung's corporate representative on the topic of JEDEC standardization of memory modules confirmed that the text on page 147 of EX1091 reflects a JEDEC proposal by Samsung. EX1090, 86:18-86:23.

> **Serial Presence Detect:**
>
> Byte 5 of the standard serial presence detect (SPD) describes the number of ranks of memory installed on the RDIMM. A rank of memory is defined as the collection of SDRAMs driven by a given rank select signal, S0 through S3. SPD byte 5 of a 4 rank RDIMM will contain the value 0x04.

The witness, who was also the presenter, vehemently disagreed that a rank of memory could include a single DRAM:

> Q: Sir, this statement is incorrect; the accepted definition of rank in 2007 or 2008 in the concept of DRAM memory modules includes a single DRAM; correct?
>
> A: ***No, that's not right***.

Id., 87:1-17 (objections omitted). This testimony is highly relevant because The '912 patent is direct to JEDEC-style memory modules. Brogioli, ¶19 (noting that a POSITA would recognize that 128Mbx8, 64Mx8 DRAMs and x64/x72 modules mentioned in the '912 patent are JEDEC-style DRAMs and modules); EX1001, 1:35-2:34, 4:42-5:5.

Dr. Wolfe agreed in IPR2022-01427/28 that "a rank is a collection of DRAMs that respond a common memory command simultaneously," but argued that devices in a rank could do a partial read. EX2056, 36:2-10. The testimony nevertheless confirmed the understanding that a rank includes multiple devices. Brogioli, ¶115.

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    Q.   Okay.  I thought a rank is a collection of
DRAMs that respond to a common memory command
simultaneously.  That's not your understanding of
what rank is?
         MR. CHANDLER:  Objection.  Form.
         THE WITNESS:  That is my understanding.
But I think in common usage, one would still call
something a rank if it had that capability but also
had the capability to do a partial read.
```

Micron's website notes that the term "ranks" "are specific to memory modules and refer to ***a sub-array of multiple*** DRAM components":

> - What is the difference between a "bank" and a "rank?"
>
> Banks are specific to individual DRAM components and refer to sub-arrays within the DRAM component. Ranks are specific to memory modules and refer to a sub-array made of multiple DRAM components.

EX2058, EX2107 (Micron FAQs), 2; *see also* EX2112, 1 (Micron-brand Crucial: "A rank is a data block that is 64 bits wide"); EX2113 (college lecture notes defining "rank" as "a collection of ***DRAM chips*** that work together with respect to request and keep the data bus full").

C. The Extrinsic Treatise Cited By Petitioners Does Not Support a Different Construction

As noted above, the intrinsic record does not support a construction of rank as including a single device. Likewise, Petitioners' extrinsic admissions in the context of JEDEC memory modules, which is the subject of the '912 patent, also do not support a construction of rank as including a single device. The Jacob textbook's disclosure does not suggest otherwise. The institution decision observed that EX1033 sets forth two potential definitions of the word "rank": "(1) a 'bank' of one or more DRAM devices that operate in lockstep in response to a given command"; and (2) "a set of DRAM devices that operate in lockstep to respond to a given command in a memory system." EX1033, 413.

10.2.2 Rank

Figure 10.5 shows a memory system populated with 2 ranks of DRAM devices. Essentially, a *rank* of memory is a *"bank"* of one or more DRAM devices that operate in lockstep in response to a given command. However, the word *bank* has already been used to describe the number of independent DRAM arrays within a DRAM device. To lessen the confusion associated with overloading the nomenclature, the word *rank* is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory system.

(EX1033, 413).

Figure 10.5 mentioned immediately before the first statement shows four devices per rank. *See* EX1033, 413.

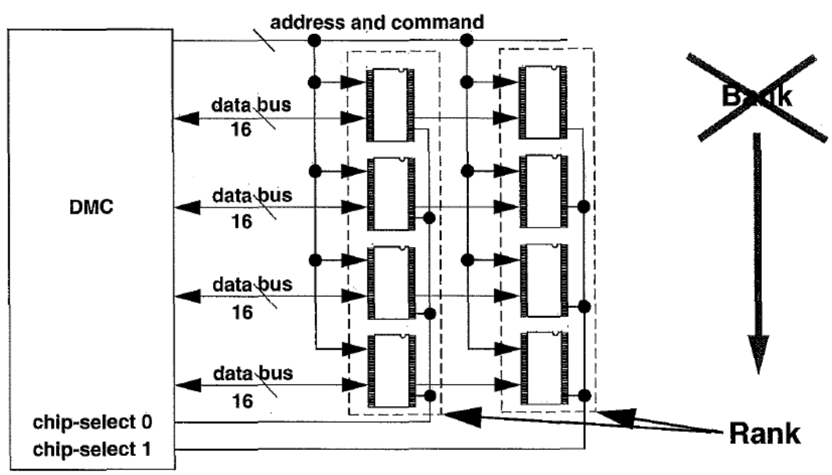


FIGURE 10.5: Memory system with 2 ranks of DRAM devices.

Jacob states because "the word *bank* has already been used to describe the number of independent arrays within a DRAM device," the term "rank" is used "[t]o lessen the confusion." *Id.* Hence, EX1033 provides that "the word *rank* is ***now used***

to denote a set of DRAM devices that operate in lockstep to respond to a given command." *Id.* That is, it is the second statement that conveys the understanding of the term "rank" at the time of invention. That definition of "rank" mentions only "a set of DRAM device***s***," and hence ***excludes*** a single-device "rank." EX1033 later also notes that "a DRAM memory module can be organized as multiple ranks of DRAM devices on the same memory module, ***with each rank consisting of multiple DRAM devices***." EX1033, 421; *see also id.*, 318 ("Each rank is ***a set of DRAM devices*** that operate in unison"), 319 Fig. 7.5 ("Each rank is a set of ganged ***DRAM devices***").

Moreover, EX1033's reference to "operat[ing] in lockstep" would make no sense for a single-device rank, because in such a rank, there would be no other DRAM devices that operate "in lockstep" in response to a command. A single-device "rank" is also inconsistent with the rest of Petitioner's construction that require the memory devices in a rank "***act together*** in response to command signal …." Pet. 12. "Act[ing] together" again connotes multiple devices.

D. The PTAB and the Federal Circuit Decisions Require a Finding that a Rank on a DDR Module Must Include Multiple Devices

During the reexamination, the Examiner allowed claim 16 by concluding that Amidi failed to teach "transmit[ting] a command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." EX1010,

3865-67, 3904; *see also* Brogioli, ¶¶ 47-55. The Examiner thus construed a "rank" as comprising "a plurality of memory devices." The Requesters challenged the Examiner's interpretation and argued that claim 16 could cover embodiments where "'one memory device' encompasses a rank of [one] memory." *Id.*, 4442. The Board rejected that interpretation and upheld the examiner's finding. EX1011, 79-80. The Federal Circuit has confirmed the Board's findings; and the findings have become final and binding on the Board.

V. ASSERTED PRIOR ART

A. Perego-422

Perego-422 discloses a memory system with point-to-point topology including a "memory module having a buffer device (e.g., having a configurable width) isolating data, control, and address signals of the memory devices from the connector interface." EX1035, 4:38-45; Abstract; 5:35-55; 8:10-17, 8:20-26. Buffer device 350 is coupled to memory controller interface 375, which includes a "plurality of memory subsystem ports 378a-378n." *Id.*, 4:63-5:15. Perego-422's configurable width buffer device is connected to ports 378a-378n of the memory controller via a point-to-point links 320. *Id.*, 5:12-21; ID at 34 (noting that Perego-422's "memory modules 330a–330n are connected in a dynamic point-to-point configuration"). Perego-422 repeatedly and consistently emphasizes the benefits of

its point-to-point architecture over a conventional JEDEC-style bus. *See, e.g.*, 3:47-56, 4:65-5:1, 5:6-15, 5:32-55, 6:15-19, 13:49-59, 21:46-50, Figs. 3A/3B, Fig. 5A.

Perego-422's buffer communicates with the plurality of memory devices on the buffered module via channels 370. *Id.*, 5:4-6, 6:13-24, 7:65-67; Fig. 3B. In Perego-422's architecture, control/address information is transmitted to the module via packets and multiplexed with data in order to be transmitted via the point-to-point links. *Id.* 13:49-59 (configurable width interface 590 may "extract the address and control information from the data"). In the example of a "normal memory read operation," Perego-422 explains that "device 350 receives control, and address ***information*** from controller 310 via point-to-point link 320a, and in response, transmits ***corresponding signals*** to one or more, or all of memory devices 360 via channels 370," *id.*, 6:12-19. Perego-422 contrasts its buffer with a conventional RDIMM buffer. *See id.*, 6:27-30 ("By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals.").

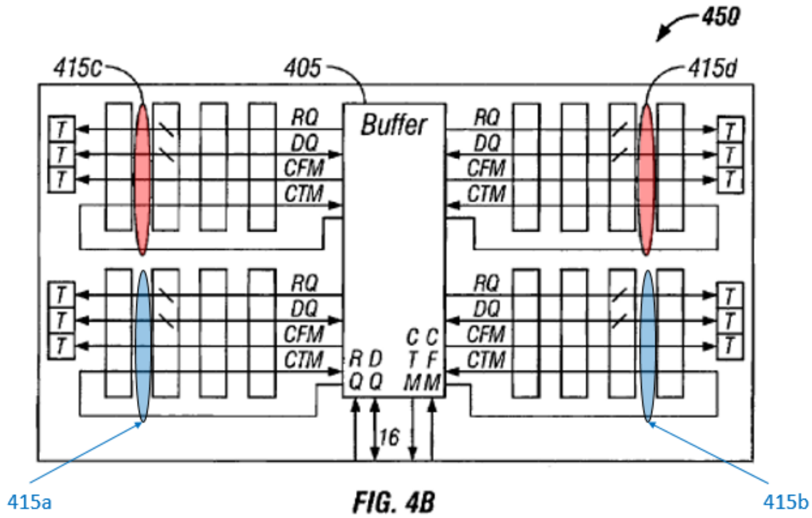


FIG. 4B

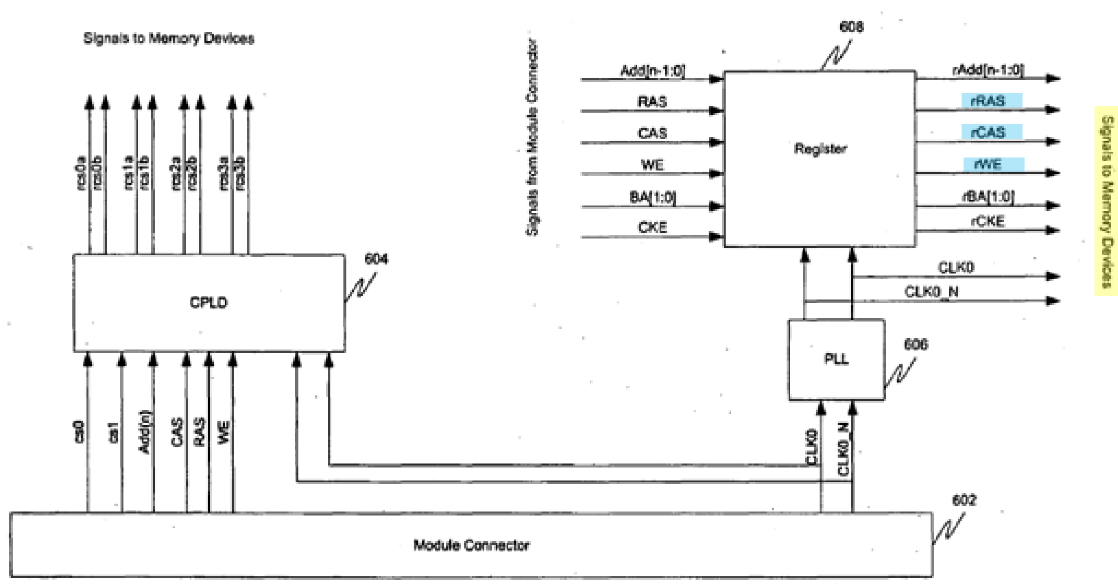
[annotated Fig. 4B]

Petitioner relies on a modified version of Perego-422's Figure 4B which Petitioner claims illustrates single-device "ranks." *See, e.g.*, Pet. 30-31, 36. Figure 4B of Perego-422 shows a memory module with multiple memory devices that communicate with the data buffer via channels (415a-415d), each of which an alleged "rank." *Id.*, 9:26-33, 10:22-36; Pet. 30; EX1003, ¶124. Perego-422 explains that in one arrangement, the channels depicted in Figure 4B operate in pairs, that is, "channels 415c and 415d are ***routed in parallel*** with channels 415a and 415b" (EX1035, 10:23-26), and in another arrangement, "channels 415a and 415b may operate ***simultaneously*** with channels 415c and 415d" (*id.*, 10:32-33). When channels operate concurrently, they would be regarded as a single rank. For instance, Dr. Wolfe explains that for the 2-channel configuration in Figure 4A, if the

channels operate concurrently, there is only a single rank of memory devices. EX2103, 198:3-8.

B. Amidi

Amidi discloses a four-rank 72-bit wide, JEDEC-style, "transparent" DDR memory module that emulates a two-rank memory module in order to "fit[] into a memory socket having two chip select signals routed." EX1036, Abstract, [0011]; *see also id.*, [0008], [0018]-[0019], [0037], [0042], Fig. 4A, Fig. 4B. Amidi purports to solve the problem that, in a conventional DRAM module architecture, the memory controller cannot access more than two ranks on the memory module because the memory controller only has two chip-selects hard-routed to the sockets of the two-rank memory module. *Id.*, [0010]-[0011].



Row Address Decoding
FIG.6A

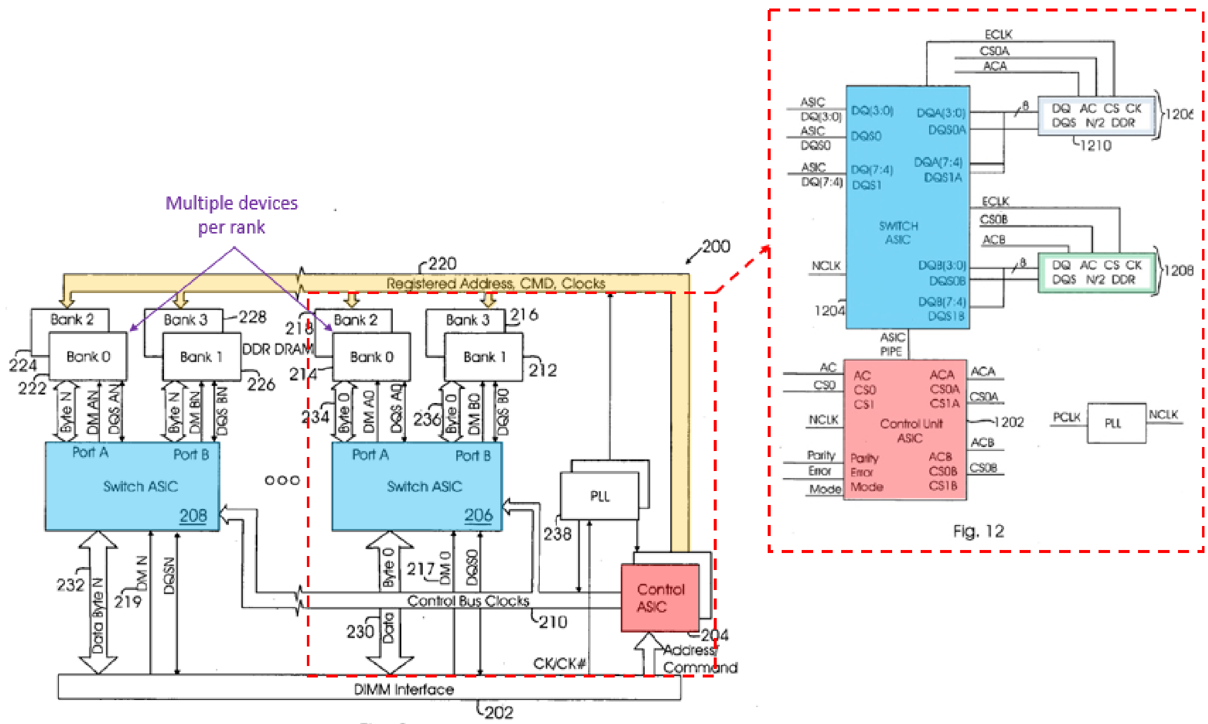
Each rank on Amidi's memory module includes "more than one memory device" per rank, *see, e.g.*, *id.*, [0008]-[0009], [0006], [0034]-[0035], Fig. 3; Fig. 4; Fig. 6A; EX2103, 173:14-19; EX1011, p.79. Moreover, Amidi teaches that the combined bit-width of the memory devices in the rank provides the bit-width of the entire rank (e.g., 64 or 72-bits). Amidi uses a traditional multi-drop bus connection with parallel signal lines for address, control and data signals. EX1036, [00029]-[0035]; Fig. 3; Fig. 6A; EX2103, 173:10-13.

C. Ellsberry

Ellsberry discloses a memory module architecture that "permits transparent bank switching of memory devices." EX1037, [0001]. As depicted in Figure 2, Control ASIC 204 (red) "receives memory addresses and commands over the DIMM interface 202" from the system memory controller, and switch ASICs 206 and 208 (purple) "receive data information from the DIMM interface 202 via data buses 230 & 232, respectively." *Id.*, [0028]-[0029]. Each switch ASIC is connected to a number of memory banks (e.g., Bank 0-3 below). *Id.* Switch ASICs 206 and 208 receive respectively data byte group N and data byte group 0, provided "simultaneously" by the DIMM interface 202. *Id.*, [0030], Fig. 2 (depicting at least two data groups); Fig. 5 (depicting nine data groups).

Figures 10-13 illustrate parts of Ellsberry's overall memory module architecture depicted in Figure 2. *See id.*, Figs. 2 and 12 (reproduced below,

annotated); EX1038, 50 (Board noting that "Figure 13 shows ***part of a memory module***"), 51, 57, 81; EX2032, 40 n.11.



[EX1037, Figs. 2 and 12 annotated]

Both of Samsung's experts contend that Ellsberry is, to at least some degree, standard-compliant.[4] *See, e.g.*, EX2103, 155:9-12 ("Q. Ellsberry deals with JEDEC compliant memory modules; is that correct? A. That's certainly within the scope of Ellsberry, yes."); *see also* EX2104 (Subramanian), 230:25-231:11 (Dr. Subramanian noting that "Ellsberry mentions standards in multiple places"). Ellsberry depicts a

[4] Given Petitioner's reliance on JEDEC standards for signaling, those need to be JEDEC compliant. *E.g.*, Pet. 72.

standard 72-bit wide memory module in Figures 5-6, consistent with JEDEC memory module standards of the day. *See* EX1037, Fig. 5, [0050] (stating its architecture is "JEDEC compatible"); EX1032 (JEDEC No. 21C), p.4.20.4-5.

But even if the memory module is not JEDEC compliant, there is no evidence that an 8-bit wide memory module of DDR devices were known at the time of the invention. *See* EX2103, 145:11-146:12, 146:22-147:6, 155:13-156:5 (Dr. Wolfe unable to identify any memory module with a bit-width of 16 or lower that featured JEDEC-compliant memory devices on it); EX2104, 258:3-259:7 (Dr. Subramanian unable to recall working with x8 or x16 memory modules with DDR2, DDR3 or DDR4 DRAMs).

VI. ON THE FULL TRIAL RECORD, GROUND 1 DOES NOT SUPPORT A FINDING OF UNPATENTABILITY

A. Perego-422 does not disclose or suggest rank multiplication

1. Perego-422 has no need for rank multiplication

Even if each channel constitutes a rank, there is no reason for Perego-422 to adopt rank multiplication because Perego-422 can use addresses to select any number of channels on the memory module. Brogioli, ¶¶138-140.

As Dr. Brogioli explains, rank multiplication is used where there are fewer chip select signals than needed to select the number of physical ranks on a memory module. Brogioli, ¶139. But that limitation does not exist in Perego-422 because Perego-422 uses "address of the transaction [to] determine which target subset of

channels 370 will be utilized for the data transfer portion of the transaction." EX1035, 14:62-65; *see also* 15:37-40 ("the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request"), 10:20-22 ("The width of the channel refers to the number of parallel signal paths included in each channel"); 10:22-36 (Perego-422 already capable of having two out of four channels or all four channels run simultaneously).

Consequently, to the extent that each channel is a rank as Petitioner asserts, there would be no need for Perego-422 to utilize rank multiplication to "fool" the memory controller into believing that there are fewer channels on a module than there actually are. Brogioli, ¶¶139-140. Perego-422's memory controller can just utilize address bits to signal which channel or channels to target. *Id.*

2. There is no substantial evidence for rank multiplication in the manner suggested by Petitioner

For Ground 1, Petitioner argues that a POSITA would have used "four ranks of low density (inexpensive) x16 memory devices in place of one rank of high-capacity (expensive) x8 memory devices." Pet. 39. As a preliminary matter, no reference in the record suggests emulating two ×n (*e.g.*, ×8) DDRs in one rank with four ×2n (*e.g.*, ×16) DDRs in four ranks as suggested here. Amidi and Ellsberry doubled the number of ranks by using devices of the same bit-widths as the emulated devices. *E.g.*, Pet. 43 (emulating 2R 128Mbx16 devices with 4R 64Mbx16 devices);

Pet. 84-85 (two 256Mbx8 devices emulating one 512Mb(x8) device). Dr. Brogioli explains the technical reasons why Samsung's approach would not be adopted, including incompatibility with x72 module formats and two virtual rank implementations, added complexity to on-module logic and routing, and significantly negative impact on data speed due to increased electrical loads. Brogioli, ¶143.

Petitioner argues that a POSITA would have used four inexpensive 32Mbx16 DDR2 devices instead of two expensive 128Mbx8 DDR2 devices to form a 2Gb memory module. Pet. 40-41. But Petitioner provides no historical data at the time of the invention to substantiate its proposal. This failure of proof is fatal, because, as Dr. Wolfe admitted at deposition, the cost difference between x8 and x16 devices "depends on the market at the time." EX2103, 91:13-15. Furthermore, to the extent cost was a major concern, Petitioner has not shown why a POSITA would have chosen four 32Mbx16 devices over four 64Mbx8 (which would lead to two ranks, each of two x8 devices): Dr. Wolfe testified that 64MBx8 could be ***cheaper*** than the 32MBx16, contrary to Petitioner's conclusory assertions that x8 devices are "expensive" and x16 devices are "inexpensive." Pet. 41; EX2103, 91:25-92:2 ("Q. So initially 64Mbx8 is actually cheaper than the 32Mbx16? A. It's ordinarily what happens.").

Petitioner also argues that it was a trend at the time to increase DRAM data width. Pet. 39. But the same article Petitioner cites to support that argument (EX1034) states, immediately following "Increase DRAM Data Width," the need to "Increase Module Data Width." EX1034, 20. EX1034 further states "the DIMM bandwidth is more important than the bandwidth of an individual DRAM." *Id.*; Brogioli, ¶146 (for improved throughput, module bit-width, not device bit-width, controls). Yet, Petitioner suggests that a POSITA would have reduced the module width from the then standard 64 bits to 16 bits, in contradiction to the very evidence it relies on.

Petitioner also argues that using four 32Mbx16 DDR2 would save power consumption. Pet. 41. The cited evidence does not support that conclusion. EX1035, 15:40-45, for example, discloses saving power by "addressing a subset of secondary channel signal lines per transaction," not using x8 versus x16 devices. Brogioli, ¶147. The cited portions of EX1036 and EX1029 do not even mention power usage; and EX1036 discusses devices of the same bit widths (EX1036, [0046]-[0048]). Brogioli, ¶147. The improperly incorporated testimony by Dr. Wolfe, even if considered, is deficient because it just considers the number of devices used per access cycles, but does not consider (1) power consumption per x16 device versus per x8 device and (2) the power consumption by devices not participating in the access cycle. Brogioli, ¶147. For example, a 512MB module

made from 64Mbx8-667 and a 2GB module made from 256Mbx4-667 devices have the following current values (EX2057, pp.14, 18):

	Precharge standby current (mA)	active burst write current (mA)	active burst read current (mA)
512MB made from 64Mbx8-667	450	1530	1620
2GB made from 256Mbx4-667	360	1215	1215

Assuming that a 2GB module made from 64Mbx8 would have the same active standby and write/read current, then for a 2GB module the total current in a write cycle would be 1530mA*n + 450mA*3n=2745n (n is the number of devices per rank). Brogioli, ¶¶148-150. In contrast, for the 2GB module made of x4 devices, the total current in a write cycle would be 1215mA*2n, less than 2745n. *Id.* Hence, it is not the case that using twice the devices in a read/write cycle would necessarily result in higher power consumption. *Id.*

B. Under the Correct Construction of "rank," Petitioner's Single-Device Constructs Are Not "ranks" [16.b.i]/[16.c.ii]

Claim 16 requires a "plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ***ranks***," and "a second number of DDR memory devices arranged in a second number of ***ranks***," EX1001, p.44, 3:9-43; [16.b.i], [16.c.ii].

The Petition's analysis relies on a construct having just one DDR per rank. *See* Pet. 30-32, 43, 52, 54, 57, 62 (relying on modified single-DDR ranks). Thus, the Petition has not shown how the limitations would be met if a rank must include multiple devices.

The Petition also fails under Petitioner's own construction. Petitioner does not deny that Perego-422's implementation would involve numerous instances with multiple devices per rank, *e.g.*, as the data access width is varied for different accesses. *See*, *e.g.*, EX2064 at 25 (64-bit wide rank); EX1035, 10:22-36, 14:16-31. But like the requesters in the '912 re-examination, Petitioner has not shown "why one skilled in the art would transmit a command signal to ***only one DDR memory device at a time when there is a plurality of memory devices in a rank***." EX1011, 79. Nor does it contend this could be done. Claim 16 is not satisfied by sending a command signal to only one DDR in a rank when the rank happens to have just one device; it requires at least the capability to send commands to only one DDR when there are multiple devices per rank. *See* EX1001, cols. 17-19 (Example 2 Verilog code showing sending command to one DDR via FET switches a and b); Brogioli, ¶¶36-43 (explaining operation of Verilog).

C. Perego-422's "channels" Do Not Constitute a "rank" Under Petitioner's Construction [16.b.i]/[16.c.ii]

Petitioner has also not shown that Perego-422 discloses "ranks" under its own proposed construction.[5] Specifically, Grounds 1 and 2 rest on modified Figure 4B featuring four channels with one DDR each, with Petitioner interpreting each channel as one rank. Pet. 28-60; EX2103, 198:3-14 (Dr. Wolfe confirming that he is only "relying on an embodiment where ***each channel is one rank***"). Petitioner has not shown that each channel would qualify as a "rank" under its own construction for multiple reasons.

1. A DDR memory module of 16 bits and less was not known at the time of the invention

Ground 1 relies exclusively on 16-bit wide, allegedly JEDEC-compliant, DDR memory modules having one 16-bit DDR per rank. *See, e.g.*, Pet. 37, 39, 41. But there is no evidence that such DDR memory modules were known at the time of the invention. Dr. Wolfe could not recall having ever "used a memory module with DDR or newer generations of DRAMs that's 16 bit wide or below" despite his 40 years of experience in the industry. EX2103, 146:2-12; *see also* 155:13-25 (not

[5] Dr. Wolfe acknowledges that Perego-422 does not use the word "rank" and the term "bank" in Perego, 15:42-45 does not refer to "rank." EX2103, 204:16-21; *see* VI.E.1.

aware of any x8 memory modules using JEDEC compliant DDR or DDR2 devices or any articles describing such modules).

Without such evidence, Petitioner has not shown that a POSITA would have modified Perego-422 to arrive at 16-bit wide memory modules comprised of 16-bit wide DDR devices. At his deposition, Dr. Wolfe repeatedly argued that it was something that a POSITA "***could***" do (EX2103, 146:2-7, 147:14-21), but obviousness requires more: it also requires a showing of why a POSITA would have done so for Perego-422, given the lack of any evidence that such a memory module was even known. *See Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1363-64 (Fed. Cir. 2016) (it was not sufficient that searching in general was known; Petitioner needed to show that the claimed searching by phone numbers was known).

As Dr. Brogioli explains, at the time of the invention, the memory bus width on the CPU was generally 32 bits or higher, making 16-bit memory modules incompatible with the vast majority of the memory controllers. Brogioli, ¶¶163-166. Petitioner, however, does not suggest modifying memory controllers. Another drawback of Petitioner's modification is that x16 memory devices would be incompatible with 72-bit memory modules (ones having ECC), because 72 is not divisible by 16. Brogioli, ¶165. As a result, because Petitioner's proposal is incompatible with the vast majority of operations, there would be no motivation to

adopt the modification. *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 795-96 (Fed. Cir. 2021).

2. Each channel reads or writes less than full bit-width of Perego-422's memory module

Petitioner relies on a modified Fig. 4B with allegedly four ranks, "each rank having a single memory device with a 'dedicated channel.'" Pet. 30-31. Perego-422 describes two alternative embodiments for the "quad-channel module 450" shown in Figure 4B. EX1035, 10:22-46. In one embodiment, "channels 415c and 415d are ***routed in parallel*** with channels 415a and 415b" (EX1035, 10:23-26), and in "alternate embodiments," "channels 415a and 415b may operate ***simultaneously*** with channels 415c and 415d" (*id.*, 10:32-34). To the extent that Petitioner agrees with its expert that the two channels operate concurrently should be regarded as a single rank, (*see* EX2103, 198:3-8),[6] there are multiple (two or four) devices per rank in the modified Figure 4B. Brogioli, ¶¶167-170.

But if Petitioner insists that each channel is a rank, then the bit width per rank, *i.e.*, 16 bits, is less than the full bit width of the memory module, characterized by the device access width W_A. EX1035, 14:23-27 & 14:38 (memory device access

[6] The parties agree that memory devices in a "rank" must "act together in response to command signals …." Pet. 12.

width, W_A, is the "number of bits that can be accessed in a single memory device transfer operation to or from configurable width buffer device 391"); EX2103, 60:21-61:5 ("memory module bit-width" is a term "used to describe the number of bits that are communicated in a single read or write operation between the memory module and the host computer"); Brogioli, ¶168 (Dr. Brogioli agreeing that W_A, corresponding to the number of bits per read/write operation, is the width of Perego-422's module).

For example, under Petitioner's mapping involving x16 memory devices, in the embodiment where channels 415 c/d are "routed in parallel" with channels 415 a/b, each transfer is 32 bits. Brogioli, ¶¶168-170. In the embodiment where all four channels operate simultaneously, each transfer is 64 bits. *Id.*

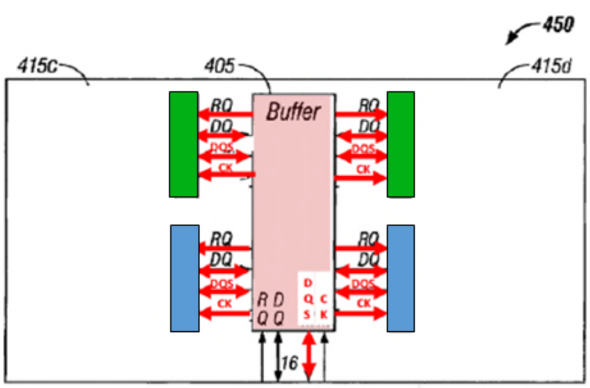


FIG. 4B

First arrangement (415c-d operate in parallel with 415a-b), 2x the device bit-width is transferred per operation

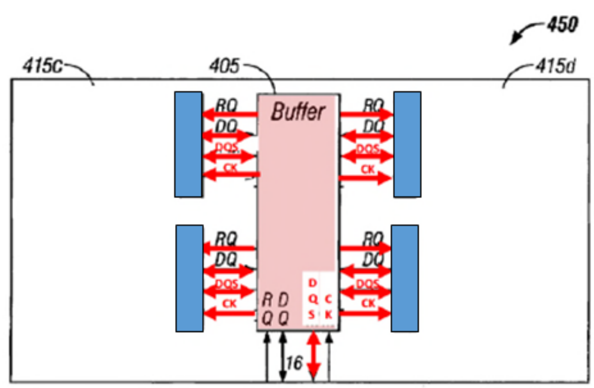


FIG. 4B

Second arrangement (all four channels operate simultaneously), 4x the device bit-width is transferred per operation

That is, the memory device access width, W_A, for Figure 4B would be either twice the per-channel bit width (first arrangement) or four times the per-channel bit widths. Brogioli, ¶¶169-170. As such, in response to a read/write operation, the memory device in each purported rank does not "read or write the full bit-width of the memory module," as required by Petitioner's own definition. *Contra* Pet. 12.

Petitioner may argue that the memory module width is W_{DP} and not W_A. *See* Pet. 31 (contending that "width of the memory module" is W_{DP} = 16.). Dr. Wolfe testified, however, that most engineers would describe the embodiment having a W_A of 128 bits and a W_{DP} of 16 bits "as a 128-bit wide memory module because that's the size of the transfers." EX2103, 61:6-14; *see also* EX2103, 56:13-21 (Dr. Wolfe confirming that W_{DP} corresponds to the number of pins on the buffer device).

Petitioner may also argue that it is relying on implementations where read and write operations each involved just one 16-bit channel, resulting in a W_A-to-W_{DP} ratio of 1. But as noted above in Section VI.C.1, there is no evidence that at the time of the invention, memory controllers operable with 16-bit wide DDR/DDR2 SDRAMs memory modules existed. As a result, a POSITA would not have modified Perego-422 to generate 16-bit wide memory modules.

In the Institution Decision, the Board noted that "a single channel is feasible" in Perego. ID at 47; EX1035, 10:14-17. However, as Dr. Wolfe confirmed, Perego-422's single-channel arrangement would have only one physical rank and is "not

practicing rank multiplication" as required by claim 16. EX2103, 53:7-54:7. Perego-422's single-channel embodiment therefore cannot render obvious claim 16.

3. Channels selected for read/write are based solely on address information

The read/write operation of the set of devices in a rank is required to be "in response to command signals, including chip select signals." *See* Pet. 12.

Dr. Wolfe admits that Perego-422 does not use the words "chip select signal" or "rank select signal." *See* EX2103, 84:14-19 ("Q. And where does the word 'chip select signal' appear in Perego? A. In one place their individual device. Let me see. I don't think there's an explicit description of a chip select line...."). Rather, in the portions relied on by Petitioner, Perego-422 discloses selecting a "target subset of secondary channel signal lines … ***via address bits*** provided as part of the primary channel request." *See* EX1035, 15:37-40; Pet. 28 (arguing "independent target subsets" or "independent banks" in Perego-422, 15:37-45 discloses "a first number of ranks"), Pet. 54; *see also* EX1035, 14:60-65 (using addresses to "determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction").

Dr. Wolfe states that "[a] chip select signal determines whether or not to pay attention to the command in a DDR environment." EX2103, 141:2-4. Petitioner does not show that those address bits are used to determine whether to pay attention

to the command in a DDR environment. In fact, Dr. Wolfe disagrees that selecting a subset of secondary channel signals is selecting a particular group of devices to respond to a single read/write request. EX2103, 202:8-10, 203:2-9. Dr. Wolfe further disagrees that the passage in 15:37-45 "specifies how ranks are selected or enabled." *Id.*, 202:8-204:10 (objections omitted):

> Q. But by selecting a subset of secondary channel signals, are you selecting a particular group of devices to respond to a single read or write request?
>
> A: I don't think so. Not in that situation. I think that that's specific to channel signal lines.
>
> ***
>
> Q. So you don't think this paragraph [15:37-45] has anything to do with grouping devices into different ranks?
>
> A: ***I do not think that this paragraph specifies how ranks are selected or enabled***.

Dr. Wolfe also clarified that the phrase "independent banks" in the passage and relied on by Petitioner (Pet. 26-27, 51) does not refer to different ranks, but "page registers which can be activated corresponding to different addresses." EX2103, 203:11-25 (objections omitted); *see* EX1034,

He confirmed that this disclosure in the preferred embodiment "simply has to do with the number of independent banks that are open at a time," not selecting or

enabling a group of memory devices constituting a "rank." *Id.*, 203:15-20. (Here, "banks" means memory arrays in a DDR device and each bank has a corresponding page register. *See* EX2103, 47:16-48:15; EX1033, p.414).

The Petition also argues that EX1035, 6:15-19 discloses "selecting 'one' memory device and transmitting … corresponding signals to the selected memory device." Pet. 37, 53. But the disclosure in 6:15-19 simply reads "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370." To the extent that Petitioner argues that a single x16 memory device can form one rank, as explained in Section VI.C.1., at the time of the invention, there were no known DDRx memory modules that were 16-bit wide or below and Petitioner has not provided any reason why a POSITA would have been interested in such a module.

Address bits are also distinct in function and organization from a "chip select signal," as Dr. Brogioli explains. Brogioli, ¶¶181-182; EX1033, p.318 ("The busses in a JEDEC-style system are classified by their function and organization into *data, address, control,* and *chip-select* busses."); *compare* EX1029, 6 ("Chip Select: ... CS provides for external Rank Selection on systems with multiple Ranks.") *with id.*, 6 ("A0 – A15 ... Address Inputs: Provided the row address for Active commands and

the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank."); EX1032, 4.20.4-6 to 4.20.4-7 (distinguishing between "SDRAM address bus" A0-A15 and "SDRAM chip select lines" S0-S3).

While, as the '912 patent teaches, address bits can be used in conjunction with chip-select signals to generate gated chip select signals (*e.g.*, EX1001, Fig. 10A), they are still different signals. Brogioli, ¶182. Interpreting "address signals" and "chip-select signals" as equivalent would render superfluous claim 16's separate recitation of "row/column address signal, bank address signals" on the one hand and "chip-select signal" on the other hand. *See* Pet. ix, [16.c.i]. Perego-422's reference to address bits therefore does not disclose or suggest reading or writing in response to a chip-select signal.

D. Perego-422's "logic element" does not receive the claimed "set of input signals" [16.c.i]/[16.c.ii]

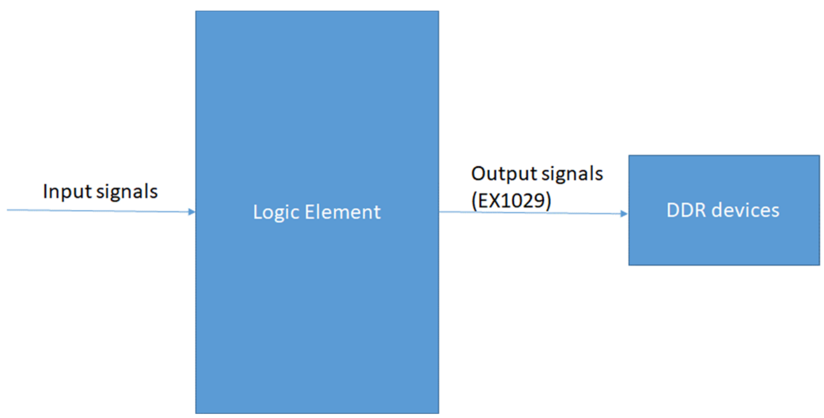
Claim 16 requires that a DDR DRAM module including a "logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal." EX1001, p.44, 3:18-22. Perego-422 does not disclose or suggest this limitation.

1. The Petition relies on irrelevant or incompatible JEDEC standards to gap-fill Perego-422's disclosure

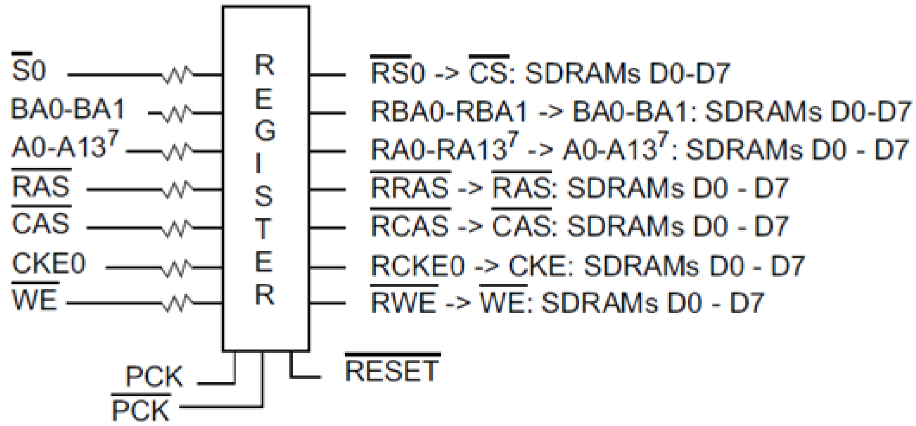
Petitioner asserts that the "set of input signals" is inherently taught in Perego-422 based on the JEDEC DDR DRAM standards (EX1029) and JEDEC DDR registered DIMM ("RDIMM") standard (EX1032). The argument suffers key deficiencies.

First, Petitioner relies on EX1029 to assert that the logic element receives "signals associated with a read or write command per the JEDEC standard." Pet. 35-36 (citing EX1029, 6, 49). But EX1029 is a JEDEC specification for DDR2 SDRAM memory devices. Where there is a buffer, as in Perego, that receives C/A information from the host and outputs C/A signals to DDR2 devices, EX1029 provides information on the C/A signals that are output from the buffer and transmitted to the DDR2 devices, but not on signals received by the buffer. EX2103, 35:12-23 (Dr. Wolfe stating "Exhibit 1029 describes the address and control protocols ***for DDR2 DRAM devices*** at the time."). Indeed, Dr. Wolfe admitted that not every utilization of a DDR2 device requires that a logic element receive the signals specified in EX1029. EX2103, 113:12-113:23 (Dr. Wolfe explaining that bank address signal must be received by the DRAM "[i]n order to use a DRAM chip such as the kind that's described in Exhibit 1029," but "[n]ot in every utilization of a DDR2 device" is it required for a logic element to receive the bank address signal).

The Petition likewise concedes that it relied on signals "for DDR memory devices," instead of those received by the alleged logic element 540. Pet. 37 (referencing address lines RQ "for DDR memory devices"). That is, Petitioner's citation to EX1029 at most shows that Perego-422's ***DDR devices***–if they are JEDEC compliant—may receive certain signals, not that the separate "logic element"—in particular the "Request & Address Logic 540" of Perego-422 would receive the recited input signals from the computer system. *See* Pet. 33 (mapping 540 to "logic element") and illustration below.



Second, for this element, the only module-level specification Petitioner cites is the JEDEC 21C standard for DDR RDIMMs, EX1032. Pet. 37; EX1032, 4.20.4-1. But Petitioner provides no evidence that Perego-422 is compatible with this cited specification. The RDIMM specification requires a register that registers C/A signals including RAS, CAS, WE, chip-select and address signals, as depicted below. EX1032, 4.20.4-11.



Perego-422 expressly distinguishes its buffers containing the logic element 540 from those "disposed on the conventional DIMM module" that were "used to buffer or register control signals such as RAS and CAS, etc. and address signals," rendering Petitioner's citations to EX1032 inapposite. EX1035, 6:27-30; Brogioli, ¶¶187-188 (JEDEC 21C standard specifies structure and operation of conventional DIMM module); EX2052 (distinguishing Rambus DIMMs from JEDEC DIMMs). Thus, EX1032 is not on point.

Nor is it inherent that the signaling received from the computer system would include the "at least one row/column address signal, bank address signals, and at least one chip-select signal," in order "to translate protocols" as Petitioner seems to assert. *See* Pet. 38. Because Perego-422 admittedly utilizes translation protocols to generate the output signals sent to the memory devices, it contemplates that the input signals would be different from the output—otherwise there would be no need for translation. Brogioli, ¶189; EX1035, 10:63-67.

Perego-422's packetized protocol relied on by the Petition differs from that described in EX1029 and EX1032 in important ways. Perego-422 states that "[i]n a normal memory read operation, buffer device 350 receives ***control, and address information*** from controller 310 via point-to-point link 320a" (EX1035, 6:15-19, cited on Pet. 51-52); and such "control ***information*** and address ***information*** may be decoded" by circuit 540 before being supplied via interface 520 to the memory devices (EX1035, 13:54-59, Pet. 36). That is, Perego-422 does not describe the signals it receives as control and address "signals," but only as "information." *See* EX1035, 6:15-19, 9:50-57, 13:49-59.

Claim 16 requires input "signals," and not input "information." EX1012, 3:18-22 ("the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal."). The specification consistently shows different lines, each dedicated to a particular type of signal, for connecting the memory controller to the logic element. *See* EX1001, Fig. 1A (lines CS_0, CS_1, A_{n+1}, Command Signals, BA_0-Ba_m), Fig. 1B (lines CS_0, A_{n+1}, Command Signals, BA_0-Ba_m), and description at 6:54-63, 7:39-49; Figs. 2A, 2B, and 20:53-21:58; Figs. 3A, 3B, and 22:15-26. There is no reference in the specification to packetized signaling or "bundling" the individually recited input signals. *Cf.* EX2103, 37:5-37:10 (Dr. Wolfe testifying that a common general definition of

"packets" is "bundles of information that are sent at different times on the same wire"). According to Dr. Wolfe, there is a distinction between a "signal" and "information" that could be contained in a signal. EX2103, 61:15-23 (Dr. Wolfe explaining that "[t]ypically, [a] signal would be something physical," while "information would be the knowledge contained in that signal.")

Dr. Wolfe confirmed that JEDEC-compliant RDIMMs at issue in EX1032 do not feature the packetized protocol cited at Petition 36 (citing EX1035, 13:54-59, Figs. 4B, 5B). EX2103, 40:20-41:11; 28:8-16 ("Q. And in the – in the traditional DIMM, is the multiplex control and address information demuxed from the data? .... No, not in a traditional DIMM that it would be compliant with JEDEC Standard 21-C [EX1032]. It would not have that characteristic."); 39:12-16 (confirming that DRAMs compliant with EX1029 "do have distinct pins for A0 through A15"); *see also* EX2103, 29:20-30:23, 30:25-31:7, 42:19-24. Simply put, Perego-422 does not disclose or suggest that its element 540 receives from the computer system signals described in EX1029 or EX1032. Brogioli, ¶193; *see also*, EX2100, 3-4 (Rambus-developed RIMM do not have specific signals for bank address or chip-select signals, only column bus and row bus signals); EX2053, p.2; EX2060, p.29 (no chip-select or enumerated address signals listed for "FBDIMM Channel Signals" received by the buffer); EX2051, pp.4-5 (no enumerated C/A signals received at the

FBDIMM connectors; instead, the information is carried on the pins for the southbound lanes), EX2116, pp.3-4 (same).

In other words, the signals transmitted from the buffer to the DRAMs can be generated by logic on the buffer based on information received from the computer system, instead of being received from the computer system. For instance, Dr. Wolfe testified that in a packetized protocol such as Rambus's, "control and address data would be broken up into chunks ... 8 bits at a time, and sent as a sequence over a limited number of wires and then ***reconstituted on the module itself into individual signals***." EX2103, 18:5-18. He admitted that signals reconstituted by the logic element and transmitted to the memory devices are "not in the same packetized form that is transmitted over the logic channel." *Id.*, 22:9-23.

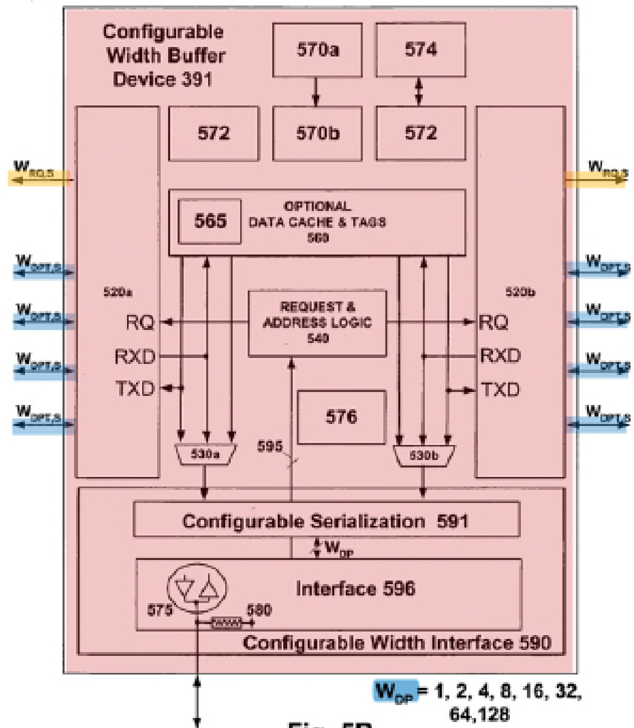


Fig. 5B

That is, the "reconstituted" signals transmitted to the DRAMs (*see* illustration above) are not the same as the "set of input signals" "from the computer system." Brogioli, ¶¶194-195. Instead, those reconstituted signals cited by Petitioner are generated internally by the circuit, and not received by the logic element from the computer system, as required by [16.c.i.]. *Id.*

2. Perego-422 does not disclose a "chip select signal"

For reasons stated in Section VI.C.3, Petitioner has also not identified any disclosure in Perego-422 of a "chip select signal" received by the buffer. *Contra* Pet. 35-36 (pointing to JEDEC standard, EX1029, as disclosing the "at least one chip-select signal").

Petitioner contends that chip-select signals are inherently present because it is "associated with a read or write command per the JEDEC standard." Pet., 33; EX1003, ¶132 (citing EX1029, at 6, 49 n.2). But the Petition relies on Perego-422's non-JEDEC compliant point-to-point configurations with configurable widths. *See*, *e.g.*, Pet. 49 (for 16.c.iii, citing to 6:15-19 that specifically mentions "point-to-point link"); Pet. 31, 34, 56 (configurable width embodiment Fig. 5b); EX2103, 43:12-20 (a JEDEC compliant memory module does not ordinarily have a configurable buffer width); *see also* EX2100, 2-5 (no chip-select pins or signals for RIMMs). Perego-422 specifically contrasts the relied-on configuration with "conventional DIMM module" that is JEDEC compliant. EX1035, 6:27-33. Moreover, even in JEDEC-specified FBDIMMs, the buffer (AMB) does not receive the enumerated set of input signals—instead, it receives commands and write data on 10 pins on southbound lanes. *See*, *e.g.*, EX2060, p.29; EX2051, p.5; EX2116, pp.3-4; *see also* EX2059, 74:19-76:6 (according to Micron's expert Dr. Stone, chip-select can be generated on memory module). On the full trial record, there is a complete failure of analysis on Petitioner's part to show that Perego-422 discloses elements [16.b.i] and [16.c.ii].

E. Perego-422 Does Not Disclose [16.c.iv]

Perego-422 does not disclose this limitation for two independent reasons: (1) it admittedly does not disclose "selecting one or two ranks …." and (2) it does not

disclose a circuit that "responds to a command signal" and "transmit[s] ***the*** command signal to at least one DDR memory device of the selected … ranks."

1. Perego-422 does not disclose selecting ranks in the claimed manner

The Petition cites 15:37-40 and 6:15-19 for alleged disclosure of rank selection. Pet. 53-55. For reasons stated in Section VI.C.3, those passages do not disclose selecting ranks in the claimed manner.

Petitioner does not cite other disclosures of "ranks" or selecting ranks in Perego-422, and provides no explanation as to how "grouping memory devices into multiple independent target subsets" discloses "rank." This failure is fatal. Dr. Wolfe's testimony that 15:37-45 has nothing to do with rank selection (EX2103, 202:8-204:10) only reinforces that Petitioner has not shown that Perego-422 discloses "ranks" or selecting ranks.

2. Perego-422 does not disclose a "circuit" that "responds to a command signal and the set of input signals" by, *inter alia*, "transmitting ***the*** command signal to at least one DDR memory device" of the selected rank(s)

Claim 16 requires a "circuit comprising a logic element and a register" in which the logic element receives specific input signals from the computer system and "wherein the circuit further ***responds to a command signal*** and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and ***transmitting the command signal*** to at least one DDR memory device

of the selected one or two ranks of the first number of ranks." Pet. ix-x. Petitioner maps the claimed circuit to the combination of Perego-422's request & address logic 540 ("logic element") and registers 597f-m ("register"). Pet. 33-35 (citing EX1035, 6:12-27, 13:54-59). Petitioner contends that [16.c.iii] is met because "[i]n a normal memory read 107 operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370." Pet. 51-52 (citing EX1035, 6:15-19).

Petitioner incorrectly assumes that Perego-422's circuit registers control/address signals are "similar to the standard registered modules of the time." Pet. 34-35. The standard RDIMMs do not receive or translate packetized input protocol to signaling protocol used by DDRx devices, as in Perego. Brogioli, ¶208; EX1032, 4.20.4-10 (depicting register of a JEDEC-standardized RDIMM, receiving control signals such as RAS, CAS, WE, and outputting registered control signals in response); *see* Section VI.D.1; EX2103, 29:20-30:23, 30:25-31:7, 42:19-24 (Dr. Wolfe unable to identify any JEDEC standards that he relied on that used the kind of packetized signaling protocol relied on in the Petition).

Indeed, Perego-422 distinguishes its buffer from the registers of a conventional RDIMM. *See, e.g.*, EX1035, 6:27-30 (distinguishing its normal

memory operation and what happens in standard RDIMMs "by way of comparison").

> With further reference to FIGS. 3A and 3B, buffer device **350** transceives and provides isolation between signals interfacing to controller **310** and signals interfacing to the plurality of memory devices **360**. In a normal memory read operation, buffer device **350** receives control, and address information from controller **310** via point-to-point link **320***a* and in response, transmits corresponding signals to one or more, or all of memory devices **360** via channels **370**. One or more of memory devices **360** may respond by transmitting data to Buffer device **350** which receives the data via one or more of channels **370** and in response, transmits corresponding signals to controller **310** via point-to-point link **320***a*. Controller **310** receives the signals corresponding to the data at corresponding ports **378***a*–**378***n*. In this embodiment, memory subsystems **330***a*–**330***n* are buffered modules. By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals. Data I/Os of the memory devices disposed on the DIMM are connected directly to the DIMM connector (and ultimately to data lines on an external bus when the DIMM is employed in memory system **100**).

(EX1035 at 6:12-30)

As discussed *supra* at 39-42, in Perego-422's packetized protocol, the control/address information transmitted from the computer system is "reconstituted" on the buffer device before being transmitted from the DRAMs. EX2103, 18:5-18; EX1035, 10:59-67 (buffer "to translate protocol employed by controller … to the protocol utilized in a particular memory device implementation"), 13:49-59 (buffer extracting C/A information from data by *e.g.*, decoding and separating C/A information from multiplexed data); Brogioli, ¶¶210-211.

Because this translation transforms serialized signals to ones suitable for use by DDR2 devices, a POSITA would understand that the request packet received by the buffer device for, *e.g.*, a read/write operation, is not "the command signals" outputted to the DDR memory devices. *Id.* Hence, Perego-422 does not disclose any "circuit" designed to "respond[] to a command signal" and "transmit[] ***the*** command signal to at least one DDR memory device" in the selected rank(s) because the request packet received by the buffer is deserialized into the signals sent to the DDR devices by the buffer. Brogioli, ¶¶210-211.

F. Perego-422 Does Not Disclose [16.d.i]

There is no substantial evidence that circuit 570a-b is operatively coupled to the register (16.d.i). The Petition argues that Perego-422, 12:65-13:5, teaches that the clock circuit 570a-b provides internal clock and synchronizing signals to the circuits within the buffer device. Pet. 59-60. But the cited disclosure merely discloses "generat[ing] internal synchronization clock signals having a predetermined temporal relationship" without disclosing to which circuits in the buffer device the signal is provided. EX1035, 12:65-13:5; Brogioli, ¶212.

Petitioner assumes that because CTM and CFM signals are exchanged with the host at the interface 590 and interface 590 allegedly includes a register, the clock circuit would be operatively coupled to the register. Pet. 59-60. But the Petition never presents any evidence that those CTM/CFM signals are sent or received by

the register. Instead, the Petition merely asserts that the register "transceives and provides isolation of address, command, and data signals between the memory controller and the memory devices on the modules…." Pet. 32. As is clear from Fig. 4B shown on Pet. 60, the clock signals are transmitted on different lines than control/address lines RQ or data lines DQ. EX1035, 9:43-53. Brogioli, ¶¶213-214. The register's coupling with RQ and DQ lines says nothing about whether it is also coupled with clock lines or the clock circuit 570a-b. As such, the Petition has simply failed to provide substantial evidence that Perego-422 discloses a PLL that is operatively coupled to the register. Pet. 59-60 (cited expert declaration merely parrots the same conclusory statement).

Petitioner argues that the limitation would be obvious by "us[ing] the functionality of Amidi's register in Perego-422 to synchronize the incoming address and control signals with the local clock signal …." Pet. 35. But that does not explain why the register should be operatively coupled with the clock signals of Perego-422: for instance, the logic element 540 which receives, translates and outputs the address and control information to the DDR devices is already allegedly coupled to the clock signals to synchronize the address/control signals with the clock signals. Pet. 35-36, 58-59; Brogioli, ¶216. Petitioner does not explain why the clock circuit should also be coupled to the register for that synchronization. Thus, Petitioner has not shown

that 16.d.i is disclosed or rendered obvious by Perego-422 alone or in combination with another reference.

VII. ON THE FULL TRIAL RECORD, PETITIONER FAILS TO ESTABLISH THAT THE CLAIM IS UNPATENTABLE OVER GROUND 2

Petitioner also argues that Perego-422 in view of Amidi renders claim 16 obvious. A POSITA would not have modified Perego-422 in view of Amidi because Amidi is not a proper IPR reference and because Perego-422 does not need the rank multiplication disclosed by Amidi. Amidi also does not cure any of the deficiencies noted for Ground 1.

A. Amidi Is Not A "Printed Publication" Under §311(b)

The AIA limits the basis for an IPR to "prior art consisting of patents or printed publications." 35 U.S.C. §311(b). Amidi is not a patent; so the question is whether it qualifies as "printed publications." It does not because it is a ***patent application*** published after the effective filing date of the invention.

Pre-AIA patent law only refers to certain art as "printed publication." In particular, pre-AIA 35 U.S.C. §102 provides that the prior art includes inventions that "w[ere]...described in a ***printed publication***…before" the invention, §102(a), or "in a ***printed publication***...more than one year prior to the date of [one's] application for patent," §102(b). The critical date for a "printed publication" is the date it is

"***published***, *i.e.*, accessible to the public." *Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1368, 1370 (Fed. Cir. 2019).

Amidi did not become a printed publication until its publication date of June 1, 2006, after even Petitioner's alleged invention date of July 1, 2005. EX1036, cover. Thus, contrary to Petitioner's assertion, Amidi does not qualify as a printed publication under §102(a). *Contra* Pet. 18.

Amidi also cannot qualify as a "printed publication" under §102(e), as that section does not even mention "printed publication" or describe a qualifying application as a printed publication before its date of publication. In IPR2023-00203, the Board found that a patent application qualifying as prior art under 102(e) is printed publication. The Board emphasized the fact that the application was "published" under section 122(b). EX2063 at 7.

But the Federal Circuit has made clear that prior art became a "printed publication" only when it became published. *In re Klopfenstein*, 380 F.3d 1345, 1348 n.2 (Fed. Cir. 2004) (quoting *In re Cronyn*, 890 F.2d 1158, 1160 (Fed. Cir. 1989) ("The statutory phrase 'printed publication' has been interpreted to mean that before the [relevant] date the reference must have been sufficiently accessible to the public interested in the art; dissemination and public accessibility are the keys to the legal ***determination whether a prior art reference was 'published***.'").

Consequently, because Amidi is a patent application published after the invention date, it does not qualify as either "patents" or "printed publications" required by §311(b). Thus, Ground 2 fails.

B. Petitioner's Combination Does Not Disclose a "logic element" that Receives the Claimed "set of input signals" [16.c.i]

Ground 2 still relies on Perego-422 for the limitation requiring the "logic element" to receive the enumerated "set of input signals." *See* Pet. 35-38 (analysis of Element [16.c.i]); *id.*, 47 (arguing that "[t]o the extent one might argue Amidi does not disclose that the 'logic 48 element' receives the claimed 'bank address signals' as part of the 'set of input signals,' Perego, alone or in combination with Amidi, teaches this"); *see also id.*, 102 (conceding "Amidi is used here only as a secondary reference with respect to a few specific limitations"). As explained above, Perego-422 does not disclose those elements; as such the addition of Amidi would not cure the deficiencies, and Ground 2 fails.

C. Petitioner Has Not Shown Why A POSITA Would Have Modified Perego-422 To Include Amidi's Ranks

As explained in Section VI.A.1, Perego-422 does not need rank multiplication because it can use address bits to select any channel of choice. *See* EX1035, 14:63-65, 15:37-40, 10:20-36; Brogioli, ¶¶138-140, 226. Amidi does not change that conclusion because, according to Amidi, rank multiplication is to address the problem of the limited number of chip-select signals that memory controllers could

provide to a standard memory module. Brogioli, ¶226; EX1036, [0010]-[0011] (describing as the "primary purpose of the present invention" resolving the need for "a transparent four rank memory module fitting into a memory socket having two chip select signals routed); [0036] (Amidi "allows the four rank memory modules to communicate with a memory socket having only two chip select signals routed."); [0041] ("CPLD 410 allows a system having a memory socket with only two chip select signals routed to interface with a four rank memory module where typically a two rank memory module couples with the memory socket.").

Perego-422, on the other hand, increases memory capacity "[b]y incorporating more channels and additional memory devices." EX1035, 10:26-31; Brogioli, ¶227. Its point-to-point architecture allows further increase in capacity by adding more modules. *Id.*, 10:36-39, 3:31-47, 5:39-44, 6:62-64; Brogioli, ¶¶227-228. Perego-422 uses addresses to select the desired channels. *Id.*, ¶228; EX1035, 14:63-65, 15:37-40, 10:20-36. And the number of modules is limited by the number of ports the system 300 has, not the number of chip-select signals that can be provided by the computer system. *See* EX1035, 5:8-15; Brogioli, ¶228. In summary, Perego-422 does not have the same problem as prior art that utilized rank multiplication—it does not rely on chip-select for channel selection and therefore its operation is not limited by the number of chip-select signals that the memory controller can send. Brogioli, ¶¶228-230. It has no need for rank multiplication. *Id.*

Furthermore, unlike Amidi which seeks to hide the actual number of ranks from the memory controller, nothing in Perego-422 suggests that it attempts to hide its number of channels from the controller. Brogioli, ¶229. Instead, Perego-422 teaches expressly that its channels can be divided into addressable subsets and be selected using address bits. EX1036, 14:63-65, 15:37-40; Brogioli, ¶229. The transparency in Perego-422 is the signaling protocol, not the number of channels (or ranks). Brogioli, ¶229; EX1036, 10:59-67 (using buffer to translate signaling protocols). Thus, a POSITA would not look to Amidi for modification because Perego-422 just does not have the same issue as Amidi. Brogioli, ¶¶229-230.

Amidi therefore does not change the fact that Perego-422 has no need for rank multiplication.[7]

[7] There is also no substantial evidence that using four 32Mbx16 DDR2 would have saved cost over two 64Mbx16 DDR2, or that it would not have been more cost effective to use two 128Mbx8 device. *Cf.*, EX2103, 91:25-92:2 ("Q. So initially 64Mbx8 is actually cheaper than the 32Mbx16? A. It's ordinarily what happens.").

VIII. ON THE FULL TRIAL RECORD, PETITIONER FAILS TO ESTABLISH THAT THE CLAIM IS UNPATENTABLE OVER GROUND 3

A. Ellsberry is Not a "printed publication" Under §311(b)

Ellsberry was not published until December 2006, after the invention date. EX1037, cover. Thus, for the same reason as stated for Amidi, Ellsberry does not qualify as a patent or a printed publication required under §311(b).

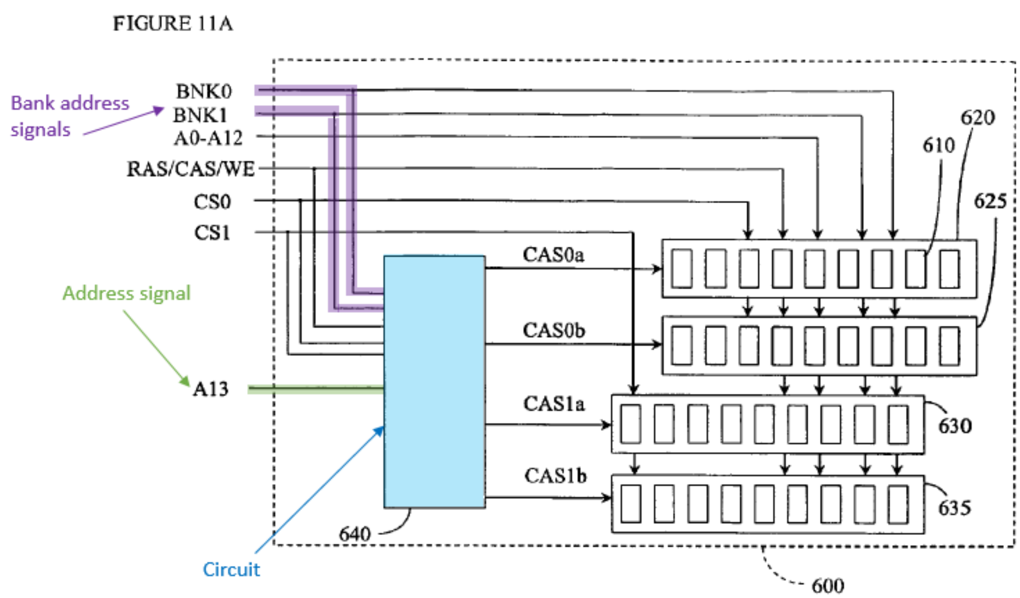
B. Ellsberry is Not Prior Art to the '912 Patent

1. The '436 patent supports the '912 patent claims

Petitioner asserts three reasons why claim 16 is not entitled to the priority date of the '436 patent. Pet. 64-67. For reasons stated below, on the full trial record written description exists for each disputed limitation.

(a) The '436 patent sufficiently describes a "circuit" comprising a "logic element" and a "register"

Petitioner argues that the '436 patent "lack[s] any embodiment including 'a circuit' comprising 'a logic element' and 'a register'…." Pet. 64. Not so. Figures 11A and 11B illustrate a four-rank DRAM module having a circuit 640 that receives address and control signals such as bank address signals BNK0 and BNK1, addresses signal A13, and command signals such as RAS/CAS/WE, CS0 and CS1 (chip-select 0 and 1). *See*, *e.g.*, EX1009, 3:5-38, 17:30-18:11.



EX1009, Fig. 11A.

The ’436 patent teaches that “the logic element [circuit] 640 comprises a programmable-logic device (PLD) 642” among other elements. *Id.*, 17:41-45. The ’436 patent further teaches that the PLD 642 in the circuit 640 “uses ***sequential and combinatorial logic*** procedures” to produce gated CAS signals or gated chip-select signals for each of the four ranks. *Id.*, 18:3-11.

Dr. Wolfe explains that ***sequential logic “describes a combination of logic functions and registers”*** because “sequential logic implements what we call state machines, which are time-variant logic functions that can perform different logic equations at different points in time based on the storage of what we call state register values.” EX2103, 117:16-118:6. As such, to implement sequential logic, one “would need both state storage in the form of a register or an equivalent, plus some

what we call combinational logic functions." *Id.*, 118:7-24. Dr. Wolfe testified that both the register and the logic functions "would somehow be present" for sequential logic. *Id.*; *id.* 118:2-13 (combinatorial logic is logic that does not store results). And that is something a POSITA would have understood in 2004-2005. *Id.*, 119:14-18. As such, a POSITA would understand that, although the '912 patent describes 640 as a "logic element," element 640 is also an example of a recited "circuit," which has a PLD 642 that includes both <u>a logic element</u> to perform the logic functions (sequential and combinatorial logic) and <u>a register to store the "state register values"</u> for the sequential logic. EX2103, 117:16-119:18; EX1009, 17:41-45, 18:3-11; Brogioli, ¶78.

(b) The '436 patent sufficiently describes "row" and/or "bank address signals"

Petitioner argues that the '436 patent also does not disclose "the claimed use of 'row' and/or 'bank address signals' as required by claim 16." Pet. 64. Claim 16, however, does not recite ***using*** row signals or bank address signals. *See* Pet. ix-x. Instead, the claim requires "the logic element receiving a set of input signals from the computer system" and the circuit containing the logic element, "generating a set of output signals ***in response to the set of input signals***." *Id.*, elements 16.c.i, 16.c.iii.

The ’436 patent provides the supporting disclosures. For example, as Figures 11A-B show, it teaches that the PLD 642 receives as inputs from the computer system, among others, a row address A13 and bank address signals BNK0/BNK1; and in response to the input signals shown to the left of PLD 642, PLD 642 outputs intermediate enabled CAS signals, which are in turn processed together with the CAS signals to cause the circuit 640 to output gated CAS signals or gated chip-select signals to access a selected rank. *See*, *e.g.*, EX1009, 17:31-34 (“To access the additional memory density of the high-density memory module 600, the two chi-select signals … are ***used with other address and control signals*** to gate a set of four gated CAS signals”); 17:34-39; 17:59-18:2 (explaining Fig. 11B), Figs. 11A-B (showing among others, address signals A13 and BNK0/1, used for generating gated output signals); 18:6-11 (instead of gated CAS signals, “[i]n certain other embodiments, the PLD 642 … uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS0a, CS0b, CS1a, and CS1b) which are each transmitted to a corresponding one of the four ranks 620, 625, 630, 635.”); *see also*, EX1011, 88 (POSITA “would have reasonably concluded that the signals that enter logic element [] have some purpose and affect the output signals”); Brogioli, ¶¶84-86. As such, the ’436 patent provides adequate written support for 16c.i-iii.

FIGURE 11A

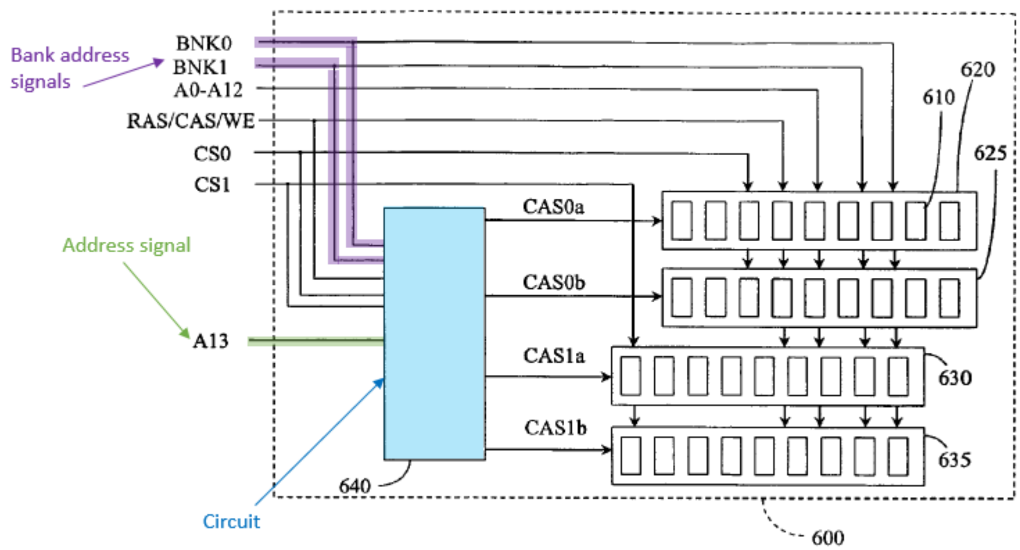
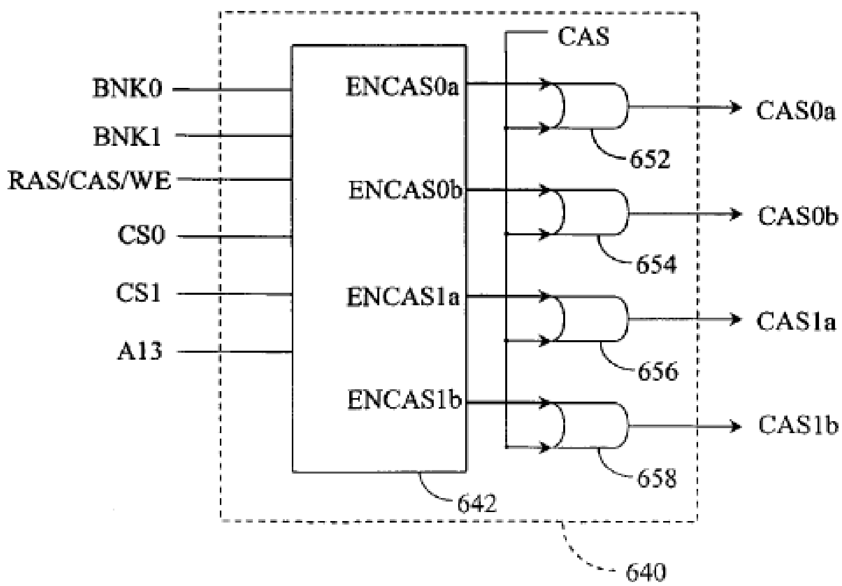


FIGURE 11B



Petitioner also suggests that Verilog is required for written support through an improper incorporation-by-reference argument. Pet. 64. That is not the law because written support does not require actual reduction to practice. *Hologic, Inc. v. Smith & Nephew, Inc.*, 884 F.3d 1357, 1361 (Fed. Cir. 2018) (test for sufficiency of

disclosure is "whether the disclosure of [earlier] application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter" as of that earlier filing date). As explained above, the '436 patent provides the written support for the limitation that the set of input signals include both bank address signals and a row address signal.

(c) Petitioner fails to show that "back to back adjacent reads" would render a rank-multiplied DRAM module inoperable

Petitioner argues that the '436 patent fails to disclose any solution to the collision problem caused by "back-to-back adjacent read commands which cross memory device boundaries." Pet. 65-66. Petitioner is incorrect.

In particular, the '436 patent claims priority to and incorporates by reference, among others, U.S. Provisional Application 60/550,668. EX1009, 1:7-12. The '668 Application (EX1006) addresses the DQS bus conflict issue caused by tying DQS pins of two devices together. EX2103, 127:5-128:16, 129:18-130:5; EX1006, [0008]-[0009], [0014]-[0015]. This results in the same bus conflict problem referenced on Pet. 65 and EX1043, 89-90, that is, when one pin is driven high and the other connected pin is driven low at the same time. The '668 Application teaches that this problem could be solved via current-limiting resistors using schemes shown in Figures 3-4. EX1006, [0016]-[0017]. Dr. Wolfe agrees that the solution would address the issues related to damage to the drivers (*i.e.*, "potentially destroy[ing] the

drivers in the memory devices" mentioned on Pet. 3). EX2103, 128:17-129:17, 130:22-24 ("1006 mitigates the physical damage issues"); *see also* EX1006, Figs 3-4 (even in worst case scenarios, the current through DRAM drivers is 34mA, less than the 50mA short-circuit current specified on p.12).

Dr. Wolfe argues, however, the solution would not address the signal error problem, *i.e.*, "whether the proper voltage level is provided at the right time in order for you to have the right alignment between the DQS and DQ." EX2103, 129:11-17, 130:6-131:8. That is, Dr. Wolfe is concerned that the voltage level might not correctly reflect the voltage needed for logic 1 and logic 0 at the right time. *Id.*

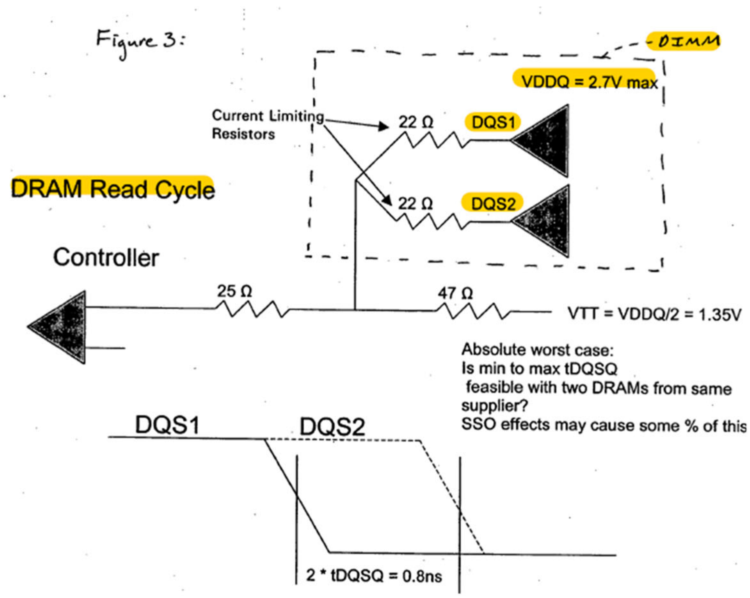
But the specific solution of the '668 Application addresses this signal error issue as well. Brogioli, ¶¶94-99. For instance, as shown in '668 Figure 4, a resistor divider network is used such that the combined DQS signal voltage level is at the mid-point of VDD (2.7V) and ground (0V), matching the voltage level of VTT (*see* table below). EX1005, p.13; Brogioli, ¶¶95-96.

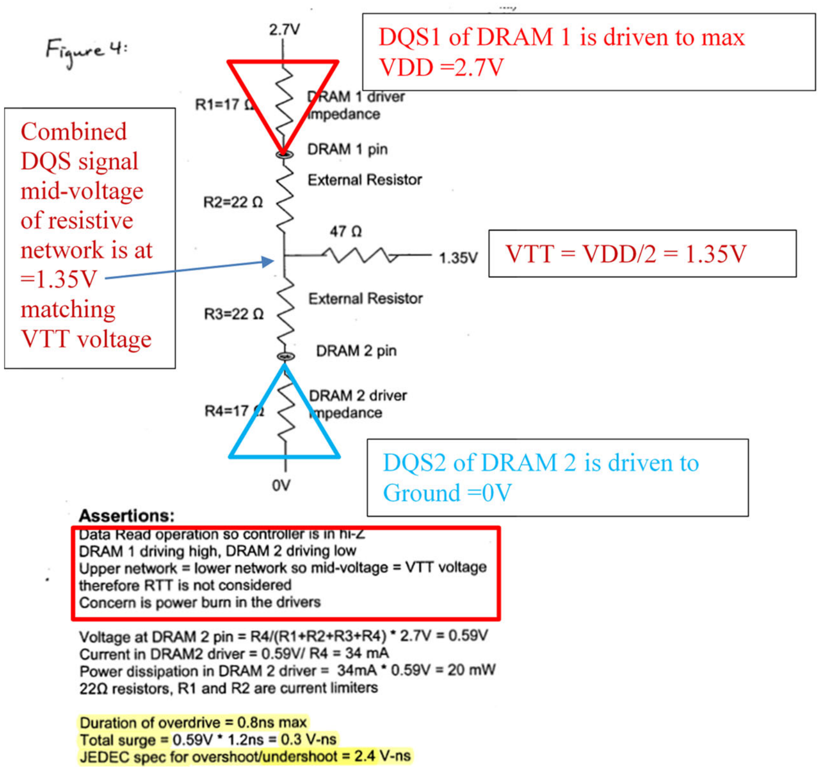
DC OPERATING CONDITIONS AND CHARACTERISTICS

Parameter	Symbol	Min		Max		Unit	Note
		D27J	D32K	D27J	D32K		
Supply Voltage	VDD	2.3	2.5	2.7	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.5	2.7	2.7	V	
I/O Reference Voltage	VREF	0.49*VDD		0.51*VDD		V	1
I/O Termination voltage(system)	VTT	VREF-0.04		VREF+0.04		V	2

This means the combined DQS signal voltage level would transition in the same way as would normally be driven by a DRAM DQS driver to overcome the

termination voltage V_{TT}, as shown in EX1006, Fig. 3 and annotated Fig. 4 below. Brogioli, ¶¶95-96.





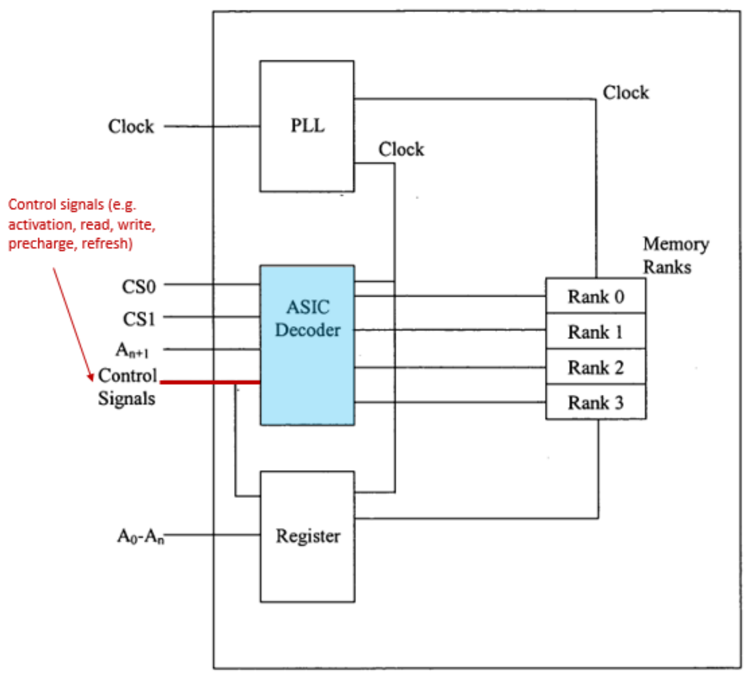
As indicated, the illustrated solution and computation example consider worst case conditions for the combined DQS signal level voltage, *i.e.*, choosing maximum operating voltage of 2.7V and choosing twice the worst case scenario for potential skew between DQS and DQ signals to account for "**variation of the output drivers for any given cycle.**" *See* EX1006, p.16, note 12; Brogioli, ¶¶97-99. The disclosed solution further specifies that due to the collision of DQS1 (=2.7V) and DQS2 (=0V) and in the extreme case when one DRAM1 DQS driver skew is at +0.4ns while the skew of DRAM2 DQS driver is at -0.4ns, the circuit of the specific solution of the '668 Application results in a maximum voltage at DRAM2 driver pin of 0.59V, which yields a total surge of 0.3V-ns for the duration of 0.8ns. *Id.* This surge level is far below the tolerance under JEDEC specification for overshoot and undershoot of 2.4V-ns. *See* EX1006, Figs. 3-4; Brogioli ¶97.

Thus, the '668 Application provides a solution via a resistive network that resolves collisions, during read operations, between two DQS signal drivers that are combined. Brogioli, ¶97. The solution solves both the combined DQS signal voltage level issue as well as the short circuit currents causing the driver damage issue. *Id.*

2. The '244 provisional supports the '912 patent claims

For the '244 provisional, the Petition's sole complaint is that it allegedly "fails to disclose a 'logic element' that receives any 'bank address' signals as required by

claim 16." Pet. 2. In its institution decision in IPR2022-00615, the Board stated that "the disclosure of 'control signals' in Figure 1 of the '244 provisional is not explicit enough to disclose the row/column address, bank address, and chip-select signals that Petitioner asserts are missing." IPR2022-00615, Paper 20 at 26. Other than bank address signals, other allegedly missing signals—chip select signals (CS0, CS1), row/column address signals (A_{n+1})—are explicitly shown in Figure 1 as being provided to the logic element (ASIC decoder). Brogioli, ¶¶59-61.



A POSITA would understand, per the JEDEC DRAM standards of the day, that the "control signals" received by the decoder ASIC (blue) for certain memory operations—such as READ/WRITE—would necessarily include bank address signals. Brogioli, ¶¶62-66.

First, Dr. Wolfe testified that in the 2000-2006 timeframe, "if [a] DRAM device was used in connection with a personal computer, then a [POSITA] would understand that a DRAM device could be a DDR2 or DDR device." EX2103, 73:9-15. The '244 application relates to memory modules for use in "a server system or a personal computer." EX1005, [0001]; Brogioli, ¶67. Dr. Wolfe further stated that "it would be ordinary for a personal computer to send CAS bar, RAS bar, WE bar, chip select signals and bank address signals to the memory module for a read and write operation at the time of the invention" and that is something a POSITA would understand. EX2103, 74:19-75:5. Hence, a POSITA viewing Figure 1 of the '244 application, given the context of usage in computer systems, would understand that the control signals would include, among other signals, bank address signals. Brogioli, ¶¶59-61, 67.

Second, a POSITA would understand that Figure 1 illustrates a JEDEC-style memory module. For instance, as co-Petitioner Micron acknowledges, "[t]he term rank was created by JEDEC ...." EX2112, 1. Figure 1 uses the JEDEC-terminology "rank", signaling that the memory module is one of JEDEC-style. *Id.* This is further confirmed by the use of chip select signals CS0 and CS1. *See* EX1005, Fig. 1; Brogioli, ¶60. According to Petitioner's evidence, a "chip-select bus, is essential in a JEDEC-style memory system[.]" EX1034, p.2. Thus, the use of JEDEC-specific terminology indicates that the '244 memory module is a JEDEC-style one. Brogioli,

¶¶60, 67; *see also* EX2103, 72:7-73:2 (Dr. Wolfe testifying that the most commonly available DDR/DDR2 devices in 2004/2005 would be compliant with JESD79 or 79-2).

Third, the Petition acknowledges that and Dr. Brogioli agrees, under the JEDEC specification, certain commands to DRAMs such as Bank Activation, Write, and Read necessarily requires bank address signals as part of the command code. Pet. 42-43 (reproduced below, annotations as in Petition); EX1029, 49 n.2 ("Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated on."); Brogioli, ¶¶63-65.

Table 10 — Command truth table.

Function	CKE Previous Cycle	CKE Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Dr. Wolfe agrees that in 2004-2005 timeframe, it "would be typical" for a conventional PC system to send, among others, bank address signals to a DIMM for a read/write operation. EX2103, 78:1-8; *see also id.*, 78:16-79:9 (signals would be sent and received, even though not used for some of the operations), 79:10-16 (in

the 2004-2005 time period, memory modules would receive chip select signals, bank address signals, CAS bar, RAS bar, write enable bar for memory operations). Likewise, the Petition states "to perform a read or write operation, the JEDEC standard … first requires ***a Bank Activate command with*** the row and ***bank address signals***, followed by ***a read or write command with the corresponding bank address signals***." Pet. 45; *see also* EX1029, 6 (bank addresses are inputted for Active, Read, Write and Precharge commands); *id.*, 49 (truth table for various commands showing the use of bank addresses); EX1030, 7 ("Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.").

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and DM signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.

(EX1029, 6)

Table 10 — Command truth table.

Function	CKE Previous Cycle	CKE Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE 3 Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 2.2.4 for details.

NOTE 4 The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 6 "X" means "H or L (but a defined logic level)".

NOTE 7 Self refresh exit is asynchronous.

EX1029, 49.

Thus, Petitioner's own evidence and statement outside the litigation context as well as testimony by its expert demonstrate that a POSITA would understand that (1) the '244 Figure 1 illustrates a JEDEC style memory module with DDR/DDR2

devices that (2) would receive from the computer system bank address signals, among others, for memory operations. Brogioli, ¶¶59-67. For the same reason, they would understand that the inventors were in possession of the concept that the bank address signals were received by the logic element. *Id.*

This is not a factual dispute. The Petition simply applies the wrong standard. Dr. Wolfe opines that "the '244 provisional does not even mention the words 'bank address' anywhere, confirming that the applicants did not have possession [of the invention]." EX1003, ¶189. That is not the law. The Federal Circuit has made clear that the specification need not recite the claimed invention verbatim. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010) (specification need not recite claimed invention *in haec verba*). Moreover, patent applications need not include and should omit that which is well known and accepted in the art. *LizardTech, Inc. v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005) ("[T]he patent specification is written for a [POSITA], and such a person comes to the patent with the knowledge of what has come before."). That the read and write commands expressly disclosed in the specification necessarily include bank address signals falls into this exact category. By ignoring the background knowledge of a POSITA, Petitioner's approach is inconsistent with black-letter law. *Capon v. Eshhar*, 418 F.3d 1349, 1357-58 (Fed. Cir. 2005) ("The 'written description'

requirement must be applied in the context of the particular invention and the state of the knowledge [in the art].”).

Finally, a POSITA would also understand that the control signal includes bank address signals because the ’244 provisional states that “two chip-select signal and one control signal (such as an ***address signal***)” can be used to generate four chip-select signals. EX1009, [0005].

> **[0005]** In certain embodiments described herein, a memory module having a first number of ranks comprises a memory module decoder. The decoder of certain embodiments comprises an Application Specific Integrated Circuit (“ASIC”) that decodes two chip-select signals and one control signal (such as an address signal) and converts them into four chip-select signals. The decoder of certain embodiments also decodes certain commands (such as refresh or precharge) that require all the ranks of memory to be active.

As shown in EX1029, address bits suitable for differentiating between two 512Mb devices emulating a 1Gb device would be BA2. *See* EX1029, p.7. Thus, a POSITA would recognize that the “address signal” mentioned in EX1009, [0005] would include BA2 and that the inventors were in possession of the claim 16 invention. Brogioli, ¶65.

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

3. Claim Chart

In IPR2023-00203, the Board indicated that Netlist needed to show support from the priority applications for each element of claim 16. Netlist presents the chart below to explain the support for each element from the '244 provisional application. Brogioli, ¶67.

'912, claim 16	**Support in the '244 Provisional**
[16.pre]	*See, e.g.*, • EX1005, [0001], [0004] [0005]-[0010], Fig. 1.
[16.a]	*See, e.g.*, • *Id.*, [0001], [0023], [0025]-[0026]

[16.b]	*See, e.g.*, EX1005, [0023], [0025]-[0026]. A POSITA would understand that the '244 application's disclosure of "DRAM" would include double-data rate ("DDR") DRAM given the application's discussion of using the memory module with general computers and reference to "rank." *See* EX2103 (Wolfe Tr.), at 72:7-14; discussion in Section VIII.B.2 above.
[16.b.i]	*See* evidence for [16.b]; *See also, e.g.*, • EX1005, [0023], [0025]-[0026], Fig. 1.
[16.c]	*See generally* disclosure related to "decoder" and "register", *e.g.*, EX1005, [0005], [0006]-[0008], [0009], [0023], Fig. 1.
[16.c.i]	The '244 Provisional provides support for a logic element (*e.g.*, "ASIC Decoder") receiving, from the computer system, the claimed set of input signals. <u>"at least one row/column address signal"</u> • EX1005, [0010] ("In certain embodiments in which the computer system supports four-rank memory modules, the ASIC uses one additional address signal (A_{n+1}) and at least one control signal."); Brogioli, ¶64 (row address needed for *e.g.*, bank activate); Pet. 45-46. • *Id.*, [0023], [0025]-[0026]. <u>"at least one chip-select signal"</u> • *Id.*, [0005], [0009], [0023], [0025]-[0026].

<u>"bank address signals"</u>

See, e.g., EX1005, Fig. 1 (illustrating "Control Signals" that can include "an address signal"), [0005] ("The decoder …comprises an … ASIC that **decodes two chip-select signals and one control signal (such as an address signal) and converts them into four chip-select signals**. The **decoder** of certain embodiments also **decodes certain commands (such as refresh or precharge)** that require all the ranks of memory to be active."), [0009], [0010]("Exemplary control signals…[to] control functions including… refresh, precharge, and other operations used for the proper functioning of the memory module."), [0011] (logic table for selecting ranks, illustrating that ASIC Decoder's I/O signals include "control signals that **defines operations**" to be performed by the memory module of Figure 1); [0019] ("**Control**" in Table 1 below "**represent[s] the various commands** that a DRAM device can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh")

Table 1:

Input signals to ASIC Decoder

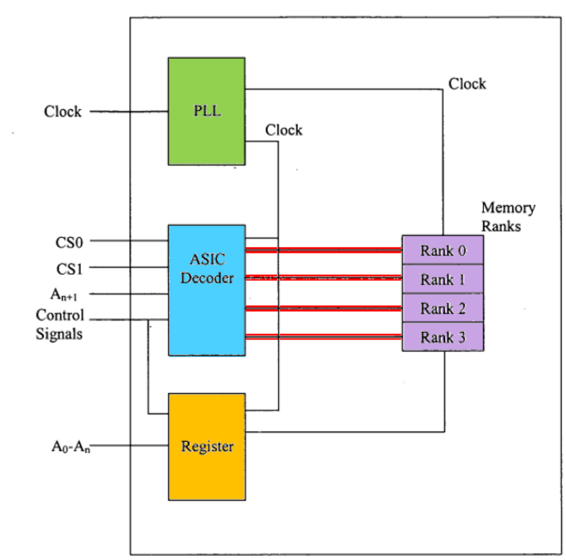
Four Output Signals From ASIC Decoder, one for each of the 4-Ranks

State	CS0	CS1	A_{n+1}	Control	RS0	RS1	RS2	RS3
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS0, CS1, RS0, RS1, RS2, and RS3 are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Control involves a number of control signals that define operations such as refresh, precharge, and other operations.

EX1049, 49 & n.2 (control signals for precharge, activate, read and write all include "BA" or bank address signals for "determin[ing] which bank is to be operated on") (cited on Pet. 45-46); EX1030, 7 ("Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being

	applied."); EX2112, p.1 ("The term rank was created by JEDEC …."), suggesting to a POSITA that 244 disclosed JEDEC-style DIMMs and DRAMs. *See also*, • [0001] (disclosing DRAM memory modules for use with "a compute system"); EX2103, 73:9-15; 74:19-75:5; 78:1-8; 78:16-79:9 (A POSITA would have understood that a DRAM device used in connection with personal computers would receive bank address signals for a read or write operation).
[16.c.ii]	*See, e.g.*, • EX1005, [0023]-[0026] (describing rank multiplication embodiments).
[16.c.iii]	*See* evidence cited for 16.c.ii. *See also, e.g.*, EX1005, Fig. 1 (depicts the circuit (ASIC Decoder + Register) receiving, as input, a set of input signals, and outputting signals to "Memory Ranks" Rank 0 – Rank 3). Figure 1: 

<table>
<tr><td>[16.c.iv]</td><td>

See evidence cited for 16.b, 16.c.ii.-16.c.iii.

See also, e.g.,

- EX1005, [0011]-[0012]-[0017], [0019] (various logic states where commands are selectively sent to ranks corresponding to RS having a value of "0").

Table 1:

<table>
<tr><th>State</th><th>CS0</th><th>CS1</th><th>A_{n+1}</th><th>Control</th><th>RS0</th><th>RS1</th><th>RS2</th><th>RS3</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Active</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>2</td><td>0</td><td>1</td><td>1</td><td>Active</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>3</td><td>0</td><td>1</td><td>x</td><td>Active</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4</td><td>1</td><td>0</td><td>0</td><td>Active</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>5</td><td>1</td><td>0</td><td>1</td><td>Active</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>6</td><td>1</td><td>0</td><td>x</td><td>Active</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>7</td><td>1</td><td>1</td><td>x</td><td>x</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>

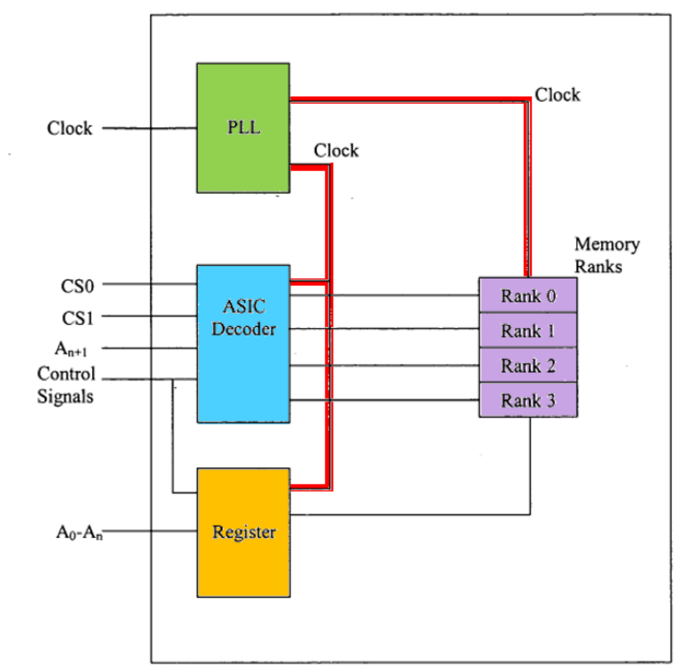
</td></tr>
<tr><td>[16.d]</td><td>

See infra, evidence cited for [16.d.i].

</td></tr>
<tr><td>[16.d.i]</td><td>

Figure 1:

Figure 1:



A POSITA would understand that the PLL is "operatively coupled" to each of these components because the PLL is coupled to each of these components

</td></tr>
</table>

	and each of these components requires a clock signal to operate. *See* Brogioli, ¶67; EX1005, [0009] (PLL "***provides the clock signals to the ranks of memory, the register, and the ASIC decoder.***").
[16.e]	*See, e.g.*, EX1005, [0019] (*e.g.*, "the control command (e.g., read) is sent to only one DRAM device or the other DRAM device so that data is supplied from one device at a time.").

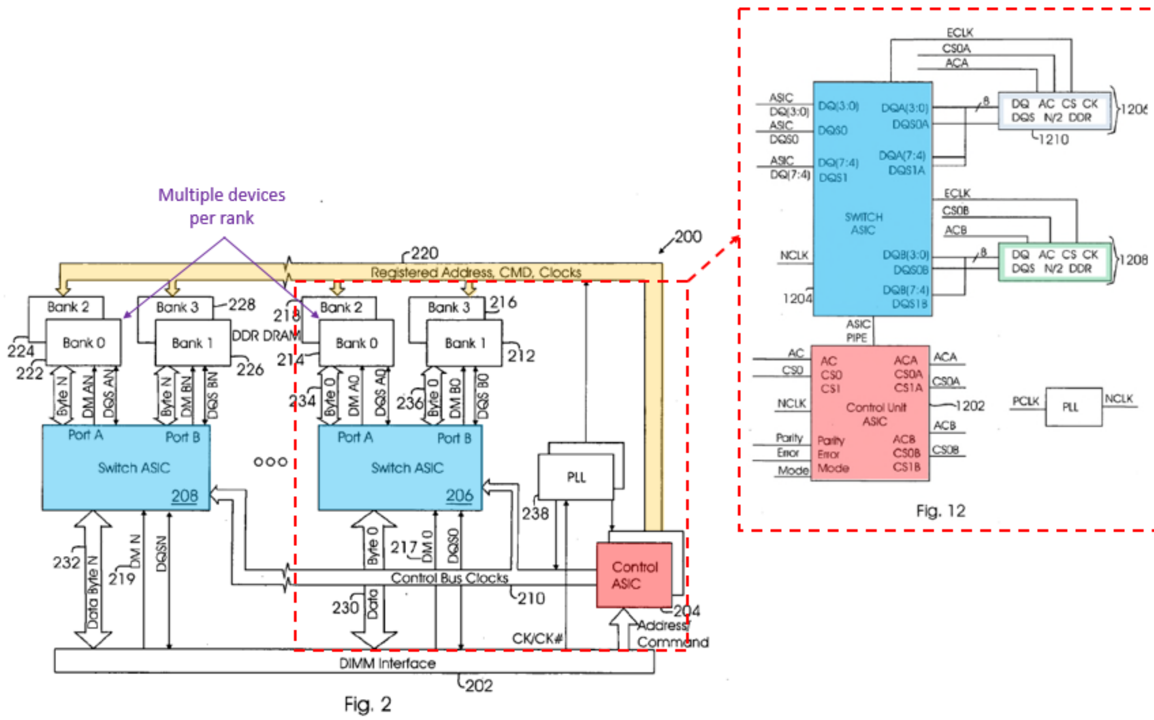
C. Ellsberry Does Not Disclose or Suggest Single-Device "ranks", and Thus Does Not Transmit a Command Signal to "only one DDR memory device" [16.e]

Even if the Board concludes that Ellsberry is prior art, Ground 3 should still be rejected on the full trial record. Petitioner acknowledges that the Board previously "found that each of Ellsberry's multiple (M) data groups simultaneously output or receive one byte (n=8 bits), thus acting on the full bit width (N=Mxn) of the module." Pet. 74. Because multiple data groups act together to read/write full bit width of the memory module, there are multiple devices per rank. Brogioli, ¶¶238, 241, 249.

But Petitioner then argues that Ellsberry's Figure 12 shows "a memory module which is eight bits wide and has two 8-bit wide ranks…." Pet. 75. The Board likewise treated Figure 12 as disclosing a complete module in IPR2023-00203. EX2063, 10-11. That is incorrect. Brogioli, ¶239.

Although Ellsberry describe Figures 10-13 as illustrating "different configurations of memory modules (e.g., DIMMs) that can be built" using its

disclosures, (EX1037, [0021]), a POSITA would not understand this to mean Figures 10-13 each illustrate a memory module, but that they each depict a different configuration for one data group of the memory module. Brogioli, ¶240.



(EX1037, Fig. 2 as compared to Fig. 12)

Figure 2 of Ellsberry illustrates "Data Group 0 through Data Group N" being provided "simultaneously." EX1037, [0030]; *see* annotation above. Each data group involves a memory device. Brogioli, ¶241. That is, each "rank" of Ellsberry would include multiple switch ASICs and the associated memory devices. *Id.*, Fig. 2 (showing two each of "Bank 0" through "Bank 3" with the rest (N=1 through N-1) omitted for simplicity); *see also* [0035] (referencing memory banks coupled to switches 206 and 208, implicating multiple data groups and hence multiple devices

per full-bit-width of the memory module); Brogioli, ¶241. Figure 2, however, does not provide details on how each switch ASIC is connected to the different memory banks, and Figures 10-13 provide that detail. *Id.*

The conclusion is consistent with other parts of Ellsberry. For instance, Figure 6 of Ellsberry illustrates "four banks of five hundred and twelve (512) megabits (Mbit) memory device 606, in a dual stacked configuration" that "appear to the system processor as 2 Gbit DRAM devices." EX1037, [0051].[8]

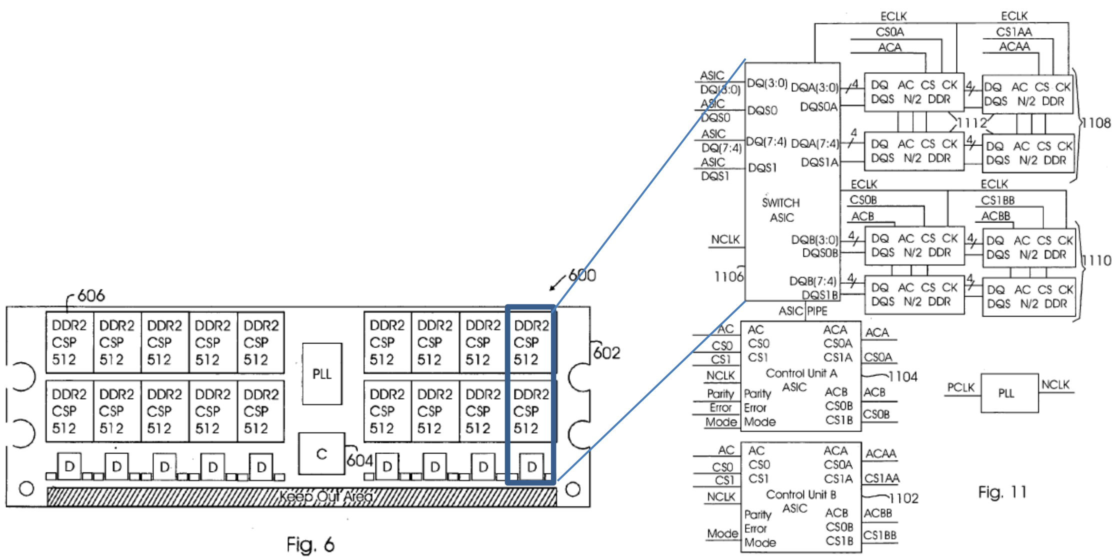


Fig. 6

Fig. 11

Figure 6 shows multiple data groups per rank. The module in Figure 6 uses a configuration "similar to that illustrated in Fig. 11" (EX1037, [0051]) even though Figure 11, like Figure 12, shows only a single bank switch and one data group. Brogioli, ¶¶242-243. Thus, a POSITA would understand that Figures 10-13 are used

[8] In Figure 6, each side of the memory module has a control unit. [0051].

to illustrate how each data group and each data switch on the memory module can be implemented, and not how many data groups the memory modules are to have. *See, e.g.*, EX1038, 50 (noting "Figure 13 shows ***part of a memory module***"), 51, 57, 81; EX2061, 40 n.11 (agreeing with Samsung that "FIGS. 2, 5, and 13 of Ellsberry correspond to a 'First Embodiment' utilizing four ranks, each composed of nine 8-bit memory devices for a total bit width of 72"). Indeed, as the Board previously noted, "in reference to Figures 10, 11, 12, and 13, Ellsberry states '[t]hese configurations employ the control unit and bank switch previously described,' ***thus relating these figures to the earlier-described control units and switches*** (including Figures 2, 5, and 6).'" EX1038, 77 (citing EX1037, [0052]). But each of these earlier-mentioned memory modules has multiple data groups and hence multiple devices per rank. *See* EX1037, Figs. 2, 5-6; Brogioli, ¶244.

This understanding would be consistent with the state of the art. Dr. Wolfe testified that he did not recall having ever "used a memory module with DDR or newer generations of DRAMs that's 16 bit wide or below" despite his 40 years of experience in the industry. EX2103, 146:2-12; *see also* 155:13-25 (not aware of any x8 memory modules using JEDEC compliant DDR or DDR2 devices or any articles describing such modules). Another expert of Samsung, Dr. Subramanian, also testified that he could not recall any memory module—regardless of JEDEC compliance—that was/is 8-bit or 16-bit wide. EX2104, 258:3-259:7.

A reference is to be interpreted from the perspective of a POSITA and their knowledge. The evidence is that at the time of the invention, there were no known eight-bit-wide memory modules, especially JEDEC-style ones, with the claimed DDRx devices on them as Petitioner now contends. EX2103, 146:2-12, 155:13-25; EX2104, 258:3-259:7; Brogioli, ¶¶245-246. Indeed, going from the standard 64-bit modules to 8-bit one would be going against the alleged industry trend of increasing module data width (*i.e.*, "Go Wider, Not Faster"). EX1034, p.20-21.

The Board questioned whether Ellsberry needed to comply with JEDEC. *See* EX2063, 12. But Ground 3 relies on implementations that "follow[] the JEDEC standard." Pet. 93; *see also* EX1037, [0050], [0057]. There is no substantial evidence that a JEDEC-compliant memory module would have a single device per rank.[9] EX1029, for example, illustrates that the per-device bit width is x4, x8 or x16. *See* EX1029, pp.1-3; *see also* Pet. 69-111 (citing EX1029 DDR2 SDRAM specification repeatedly), Pet. 73 (citing EX1032 DDR SDRAM RDIMM Specification). EX1032, a module-level specification, requires 64- or x72-bit wide

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[9] Co-Petitioner, Micron, acknowledges that the term "rank" "was created by JEDEC …." EX2112, 1. Hence, claim 16 implies a JEDEC-style memory module with DDR devices whose full bit-width is x64 or x72 (ECC). *See* EX1032, p.4.20.4-5; EX2049, p.4.20.6; EX2050, p.4.20.2-5; Brogioli, ¶247, n.9.

memory modules. EX1032, p.4.20-4.5 ("DIMM organization" "x72 ECC, x64"). This means that there are eight or nine x8 devices per rank. Brogioli, ¶247; EX2103, 46:3-15 (a 64-bit wide memory module would have, respectively, sixteen x4 DRAM devices, eight x8 DRAM devices, and four x16 DRAM devices, per rank); EX2112, 1 (Micron stating "[a] rank is a data block that is 64 bits wide"); EX1090, 86:19-87:17 (Samsung corporate witness denies that a rank could include a single DRAM).

Ellsberry also aims to "expand[] the memory capacity of a memory module." *Id.*, [0010], title. Reducing the number of devices per rank (to one device per rank) would reduce rather than expand the capacity of the memory module. Petitioner argues, however, that [0035] suggests "that the configuration can, but is not required to, be expanded to several data groups." Pet. 76. But [0035] actually references ***two*** switch ASICs corresponding to ***two*** data groups:

> The control unit 204 then handles mapping the logical memory addresses it receives via the DIMM interface 202 to a corresponding bank for a particular memory bank coupled to the ***switches 206 and 208***. This same principal is expanded when implementing a wider memory bus formed by several data groups composed of a plurality of memory bank switches and the associated memories. EX1037, [0035].

Brogioli, ¶¶248-249; *see also id.*, [0030] (noting that "***a first data group*** … is received by ***bank switch 206*** while a ***second data group*** … is received by ***bank switch 208***"). Thus, consistent with Figure 2's illustration of Ellsberry's overall

architecture, Ellsberry's memory modules have multiple devices per rank. EX1037, Fig. 2.

Petitioner also points to Perego-422's configurable bit-width with a W_{DP} of 8 bits to suggest that a POSITA would design an 8-bit wide DDR DRAM module. Pet. 76. Dr. Wolfe testified, however, the memory device access width, W_A, not W_{DP}, corresponds to the number of bits "for a single read or write operation." EX2103, 55:4-57:4, 61:6-14. That is, W_{DP} is not the full bit-width of the memory module as Dr. Wolfe confirmed. *Id.*; Brogioli, ¶¶248-249; *see also* EX1035, 14:63-67 (selecting channels by using address bits). More importantly, Petitioner relies on Ellsberry implementations that "follow[] the JEDEC standards," and these JEDEC-style memory modules are 64- or 72-bit wide. EX1032, p.4.20.4-5; EX2049, p.3.

Petitioner also argues that it would have been obvious to make a module with only a single data group, because allegedly a POSITA would have understood that such a module "would have been simpler to make and required fewer parts, leaving fewer error sources," citing Dr. Wolfe's declaration which parrots the same without elaboration. Pet. 76. Petitioner's conclusory approach is legally insufficient. *Arendi*, 832 F.3d at 1362 ("common sense" cannot "substitute for reasoned analysis and evidentiary support, especially when dealing with a limitation missing from the prior art references specified"). The simple fact is that there is no evidence that a POSITA had ever thought of constructing an 8-bit wide DDR memory module as

Petitioner argues because it was simply not known or suitable for use with a computer system at the time, which was generally 32-bit or 64-bit wide. Brogioli, ¶251; EX2103, 146:2-12, 155:13-25 (Dr. Wolfe unaware of any x8 memory modules with DDRx devices or any articles describing such modules); EX2104, 258:3-259:13 (Dr. Subramanian not aware of any x8 memory modules with DDR's on them). Nor does it make any technical or economic sense. If simplicity is desired, Ellsberry would just couple a 1Gbx8 (or 512Mbx8) device directly with the CPU, as the cost saved by removing PCB, PCB routing, costly switch ASIC and control ASIC would more than offset any potential price difference between a single 1Gbx8/512Mbx8 and two 512Mbx8/256Mbx8 devices. Brogioli, ¶252. Simply put, Petitioner used the claims as a roadmap to piece together the modifications. That is hindsight.

IX. NO SIMULTANEOUS INVENTIONS

Petitioner claims that Amidi, Perego-422 and Ellsberry establish simultaneous invention. The Board has repeatedly considered and rejected the argument that Amidi renders obvious claim 16; the Federal Circuit agreed and the holding is binding. *Supra*, II.B. Perego-422 does not solve the same problem as the '912 patent because it does not even need rank multiplication. *Supra* VI.A. As to Ellsberry, the ground cites repeatedly to the JEDEC standard; but JEDEC-style DDR2 memory modules are 64-bit or 72-bit wide, resulting in eight or nine x8 DDR2 devices. *See*

EX1032 (x64 or x72 module widths); *supra*, VIII.C. Petitioner does not contend that Ellsberry could send a command to just one DDR device in a multi-device rank.

X. CONCLUSION

Based on the foregoing, the Board should find claim 16 of the '912 patent is not unpatentable.

Dated: August 10, 2023

Respectfully submitted,

/Hong Zhong/

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I hereby certify, pursuant to 37 C.F.R. section 42.24, that the foregoing Patent Owner Response contains 14,997 words, excluding the words in the table of contents, table of authorities, mandatory notices under section 42.8, this certificate of word count, certificate of service or exhibit list. The word count is based on the word count of the Microsoft Word program used to prepare the Patent Owner Response.

/Hong Zhong/
H. Annita Zhong (66,530)

CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. section 42.6, that on August 10, 2023, a complete copy of the **PATENT OWNER'S RESPONSE and EXHIBITS 2049-2064, 2100-2104, 2107-2108, 2110-2116** were served upon the following, by ELECTRONIC MAIL:

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